

**HP Patton X2 (HP SCH P/N:675886-000)**

BTX(213.3 mm X 266.7 mm)

(MS-7782 0B)

HP P/N	Description
675885-001	PCA, Patton
675886-000	SCH, Patton
675887-001	PCB, Patton

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**CPU:**

INTEL - Sandy or Ivy Bridge LGA 1155

**System Chipset:**

INTEL-IBEXPEAK PCH-H61

**OnBoard Chipset:**

AZALIA Codec: ALC 221

LAN: Boradcom BCM57788 10/100/1000 NIC

SIO: Nuvoton NPCD379H

PCIe to PCI Bridge: ASM1083

Flash ROM: 64 Mb

**Main Memory:**

DDR3 (1066/1333MHz) \* 2 (Dual Channel)

**Expansion Slots:**

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 1

PCI Slot \* 2

**PWM:**

Controller: NCP81005

Controller: NCP5230MNTWG

Controller: TPS51220

Controller: NCP1587DR2G

**Other:**

SATA(SATA2-300MB/s) \*2

USB2.0 \*10 (Rear\*4 Front\*4 Internal \*2)

DVI-D\*1

VGA PORT \*1

PRINT Header \*1

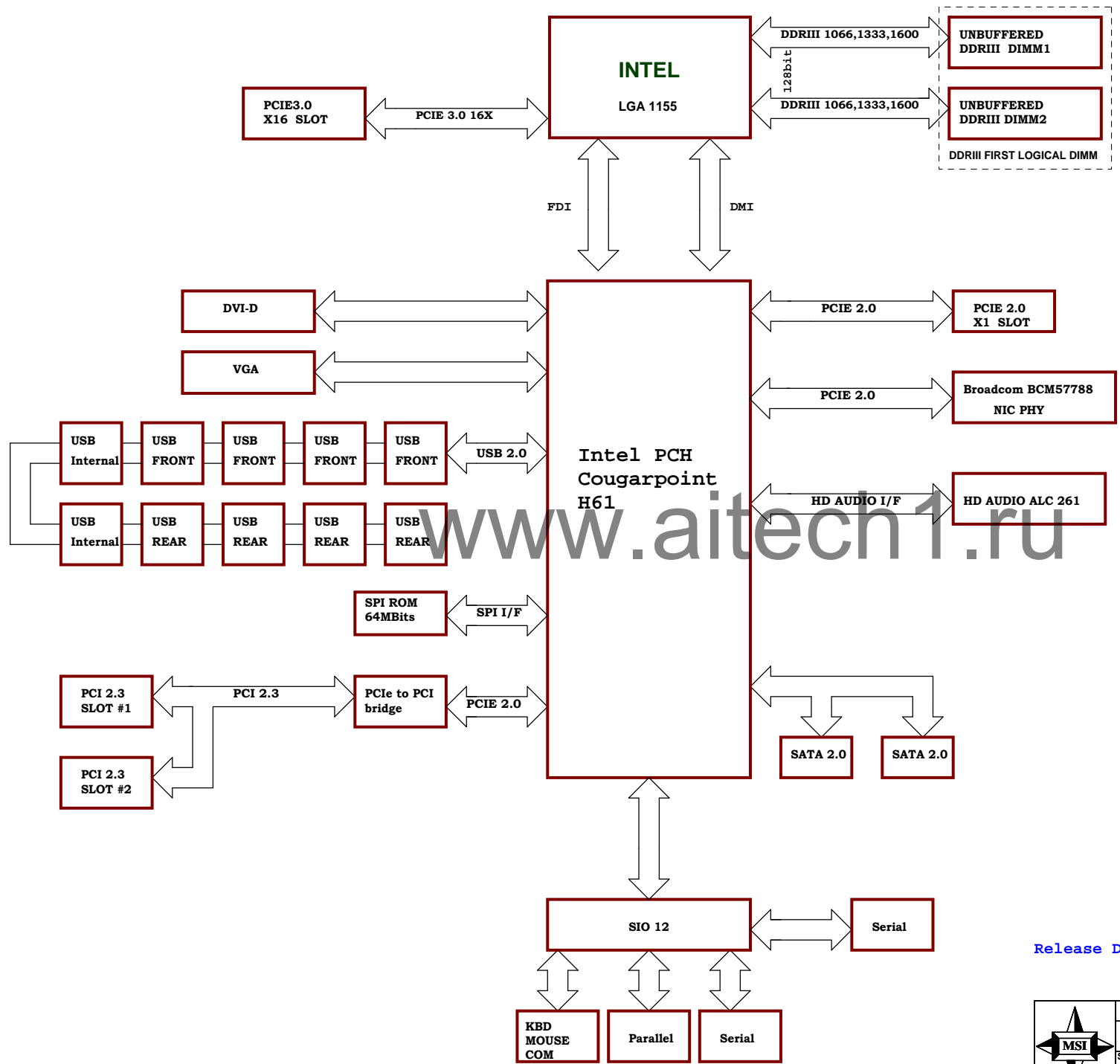
COM PORT \*1

COM Header \*1

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## DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#A PCI_INT#B PCI_INT#C PCI_INT#D	PCI_REQ0# PCI_GNT0#	AD16	CLK33M_PCI_SLOT1
PCI Slot 2	PCI_INT#B PCI_INT#C PCI_INT#D PCI_INT#A	PCI_REQ1# PCI_GNT1#	AD17	CLK33M_PCI_SLOT2
SIO				CLK33M_SIO
PCIe to PCI Bridge				CK_ASM_PCI33M


## USB MAPPING

Controller	Port	Destination	Fuse	Bulk Cap	OC#
EHCI #1	Port 0	Front I/O (P24)	SW	YES	3
	Port 1	Front I/O (P24)			
	Port 2	Media (P150)	SW	YES	0
	Port 3	Media (P150)			
	Port 4	Front I/O (P25)	SW	YES	3
	Port 5	Front I/O (P25)			
	Port 6	USB Port 6 is disabled for H61			
	Port 7	USB Port 7 is disabled for H61			
EHCI #2	Port 8	Lan +USB	SW	YES	6
	Port 9	Lan +USB			
	Port 10	Rear USB x2	SW	YES	5
	Port 11	Rear USB x2			
	Port 12	USB Port 12 is disabled for H61			
	Port 13	USB Port 13 is disabled for H61			

## PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCI_RST#	PCI SLOT1 (J20)
PCI_RST#	PCI SLOT2 (J21)
PE_X16_RST#	PCI-E SLOT X16 (J41)
PE_X1_RST#	PCI-E SLOT X1 (J31)
PE_LAN_RST#	LAN (U10)
PE_PCI_RST#	PCIe to PCI Bridge (U12)

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Pin	Default Function / Alternate Functions	Buffer Type	Buffer Power Wells	Motherboard Function
1	CLAMP_CTRL	OD <sub>8</sub>	VS <sub>B3</sub>	BLEED OFF CIRCUIT
2	SLP_S4#	IN <sub>T04</sub>	VS <sub>B3</sub>	SLP_S4#
3	SLP_S5#	IN <sub>T04</sub>	VS <sub>B3</sub>	SLP_S5#
4	SLP_S3#	IN <sub>T04</sub>	VS <sub>B3</sub>	SLP_S3#
5	SIOPME#	OD <sub>8</sub> , O <sub>48</sub>	VS <sub>B3</sub>	RI#
6	RSMRST#	O <sub>36</sub>	VS <sub>B3</sub>	RSMRST#
7	PME_IN#	IN <sub>T0</sub>	VS <sub>B3</sub>	PME status
8	BLINK_GR	O <sub>20/30</sub>	VS <sub>B3</sub>	Power LED driver
9	COLOR	O <sub>30/30</sub>	VS <sub>B3</sub>	Power LED driver
10	VSS	I	GND	GND
11	PWRGD_OUT	OD <sub>6</sub>	VS <sub>B3</sub>	PWRGD_140ms
12	PS_ON#	OD <sub>6</sub>	VS <sub>B3</sub>	PS_ON#
13	TACH1	IN <sub>T0</sub>	VDD3	SYS_FAN_TACH
14	CLOCK132	IN <sub>T0</sub>	VS <sub>B3</sub>	SUS_CLK_IO
15	3V_AUX_SLOT_ON	O <sub>48</sub>	VS <sub>B3</sub>	3V_AUX_SLOT_ON
16	VS <sub>B3</sub>	I	PWR	VS <sub>B3</sub>
17	VCORF	I	N/A	VCORF
18	LDRQ#	O <sub>PC1</sub>	VDD3	LDRQ#
19	LAD3	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	LAD3
20	LAD0	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	LAD0
21	LAD2	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	LAD2
22	VSS	I	PWR	GND
23	LAD1	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	LAD1
24	SER_IRQ	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	SERIRQ
25	PCI_RESET#	IN <sub>PC1</sub>	VDD3	PLTRST#
26	PCI_CLK	IN <sub>PC1</sub>	VDD3	33MHz
27	LFRANE#	IN <sub>PC1</sub>	VDD3	LFRANE#
28	VS <sub>B3</sub>	I	PWR	VS <sub>B3</sub>
29	GPRST3#	O <sub>14</sub>	VS <sub>B3</sub>	PCIE_X16 RESET#
30	INTRUDER#	IN <sub>T0</sub>	V <sub>BAT</sub>	HOOD_SENSE#
31	5V_USB_CTRL	O <sub>48</sub>	VS <sub>B3</sub>	5V_USB_EN
32	HDLOCK#	OD <sub>12</sub>	VDD3	HOOD_LOCK#
33	GPI001	IN <sub>T0</sub> /OD <sub>9</sub> , O <sub>48</sub>	VS <sub>B3</sub>	
34	HDUNLOCK#	OD <sub>12</sub>	VDD3	HOOD_UNLOCK#
35	HD_LED_IN#	IN <sub>T0</sub>	VDD3	Hard Drive LED Input
36	CPU_PRSTNT1#	IN <sub>T0L</sub>	V <sub>BAT</sub>	CPU detection
37	VBAT	I	PWR	

38	12V_VSB_COMP	IN <sub>COMP2</sub>	VS <sub>B3</sub>	
39	COMP_IN3	IN <sub>COMP3</sub>	VS <sub>B3</sub>	
40	COMP_IN1	IN <sub>COMP1</sub>	VS <sub>B3</sub>	5V voltage monitor
41	COMP_IN2	IN <sub>COMP2</sub>	VS <sub>B3</sub>	12V voltage monitor
42	AVCC	I	PWR	AVCC
43	AD1	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	AD1
44	AD2	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	AD2
45	AD3	IN <sub>PC1</sub> /O <sub>PC1</sub>	VDD3	AD3
46	FSPI_STR	IN <sub>T0</sub>	AVCC	FSPI_STR
47	AGND	I	GND	AGND
48	PWBTOUT#	IN <sub>T04</sub>	VLPS	PWBTOUT#
49	PWBTIN#	IN <sub>T04</sub>	VLPS	PWBTIN#
50	LPS_WAKE	IN <sub>T0</sub>	VLPS	LPS_WAKE
51	LPS_PHY#	O <sub>48</sub>	VLPS	LPS_PHY#
52	LPS_ON#	O <sub>48</sub>	VLPS	LPS_ON#
53	VLPS	I	PWR	VLPS
54	VTT	I	PWR	VTT
55	THERMTRIP#	IN <sub>AGTL</sub>	VTT	THERMTRIP#
56	TSI_SCL	IN <sub>T0</sub> /O <sub>T01</sub>	VTT	TSI_SCL
57	PROCHOT1#	IN <sub>AGTL</sub> /OD <sub>AGTL24</sub>	VTT	PROCHOT1#
58	PECI	IN <sub>PEC1</sub> /O <sub>PEC1</sub>	VTT	PECI
59	PROCHOT2#	IN <sub>AGTL</sub> /OD <sub>AGTL24</sub>	VTT	PROCHOT2#
60	VSS	I	PWR	GND
61	PWM2	OD <sub>12</sub> , O <sub>6/12</sub>	VDD3	SYS-FAN/PWM_REAR
62	HMSCL	IN <sub>48</sub> /OD <sub>6</sub>	VS <sub>B3</sub>	HMSCL
63	PWM1	OD <sub>12</sub> , O <sub>6/12</sub>	VDD3	SYS-FAN/PWM_FRONT
64	HMSDA	IN <sub>48</sub> /OD <sub>6</sub>	VS <sub>B3</sub>	HMSDA
65	HD_LED_OUT	OD <sub>16</sub>	VS <sub>B3</sub>	Hard Drive LED Output
66	WAKE_OUT#	OD <sub>12</sub> , O <sub>6/12</sub>	VS <sub>B3</sub>	Wake Disable Output
67	GPIO15(EV6#)	IN <sub>T0</sub>	VS <sub>B3</sub>	PCI_Express_Wake#
68	AMP_ON	O <sub>48</sub>	VS <sub>B3</sub>	AMP_ON
69	AMP_ON#	O <sub>48</sub>	VS <sub>B3</sub>	AMP_ON#
70	GPRST2#	O <sub>14/14</sub>	VS <sub>B3</sub>	PE_RST#_OUT
71	12V_PG_25MS	OD <sub>6</sub>	VS <sub>B3</sub>	12V_PG_25MS
72	KBDNST#	IN <sub>T0</sub> , OD <sub>14</sub>	VDD3	KBDNST#
73	AUDIO_BEEP	O <sub>48</sub>	VS <sub>B3</sub>	DIAG Beep
74	TACH2	IN <sub>T0</sub>	VDD3	TACH2
75	VS <sub>B3</sub>	I	PWR	VS <sub>B3</sub>
76	KBDAT	IN <sub>T0</sub> , OD <sub>14</sub>	VDD3	KBDAT
77	MDAT	IN <sub>T0</sub> , OD <sub>14</sub>	VDD3	MSDATA
78	SLIN_ASTRB#	OD <sub>14</sub> , O <sub>14/14</sub>	VDD3	RSLIN#
79	KBCLK	IN <sub>T0</sub> , OD <sub>14</sub>	VDD3	KBCLK
80	MCLK	IN <sub>T0</sub> , OD <sub>14</sub>	VDD3	MCLK
81	PD3	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD3
82	PD4	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD4

83	INIT#	OD <sub>14</sub> , O <sub>14/14</sub>	VDD3	INIT#
84	VSS	I	PWR	GND
85	PD1	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD1
86	PD6	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD6
87	PD0	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD0
88	PD2	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD2
89	PD7	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD7
90	PD5	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	PD5
91	STB_WWRITE#	OD <sub>14</sub> , O <sub>14/14</sub>	VDD3	RSTB#
92	ERR#	IN <sub>T0</sub>	VDD3	RERR#
93	VS <sub>B3</sub>	I	PWR	VS <sub>B3</sub>
94	AFD_DSTRB#	OD <sub>14</sub> , O <sub>14/14</sub>	VDD3	RAFD#
95	PE	IN <sub>T0</sub>	VDD3	RPE
96	GA20	IN <sub>T0</sub> , O <sub>14/14</sub>	VDD3	GA20
97	ACK#	IN <sub>T0</sub>	VDD3	RACK#
98	SLCT	IN <sub>T0</sub>	VDD3	RSLCT
99	BUST_WAIT#	IN <sub>T0</sub>	VDD3	RBUSY
100	TACH3	INTS	VDD3	TACH3
101	SMB1SDA	SW <sub>0M</sub>	VDD3	SMB_DATA_MAIN
102	PWRGD_PS	IN <sub>T04</sub>	VS <sub>B3</sub>	PWROK_PS
103	SMB2SDA	SW <sub>0M</sub>	VDD3	SMB_DATA_RESUME
104	PWRGD_O2#	OD <sub>6</sub>	VS <sub>B3</sub>	PWRGD_50MS#
105	PWM3#	OD <sub>12</sub> , O <sub>6/12</sub>	VDD3	PSU-FAN/PWM
106	5V_USB_MAIN#	OD <sub>8</sub>	VS <sub>B3</sub>	5V_USB_MAIN#
107	PWRGD_O1	OD <sub>6</sub>	VS <sub>B3</sub>	PWRGD_30MS
108	VSS	I	PWR	GND
109	SMB1SCL	SW <sub>0M</sub>	VDD3	SMB_CLK_MAIN
110	SMI#	OD <sub>6</sub>	VDD3	IO_SMI#
111	SMB2SDL	SW <sub>0M</sub>	VDD3	SMB_CLK_RESUME
112	DSR1#	IN <sub>T0</sub>	VDD3	DSRA#
113	RI1#	IN <sub>T0</sub>	VDD3	RIA#
114	CTS1#	IN <sub>T0</sub>	VDD3	CTSA#
115	DCD1#	IN <sub>T0</sub>	VDD3	DCDA#
116	SIN1	IN <sub>T0</sub>	VDD3	SINA
117	RTS1#	O <sub>48</sub>	VDD3	RTSA#
118	DTR#_BOUT1	O <sub>48</sub>	VDD3	DTRA#
119	SOUT1	O <sub>48</sub>	VDD3	SOUTA
120	DCD2#	IN <sub>T0</sub>	VDD3	DCDB#
121	SOUT2	O <sub>48</sub>	VDD3	SOUTB
122	VS <sub>B3</sub>	I	PWR	VS <sub>B3</sub>
123	DTR#_BOUT2	O <sub>48</sub>	VDD3	DTRB#
124	RI2#	IN <sub>T0</sub>	VDD3	RIE#
125	RTS2#	O <sub>48</sub>	VDD3	RTSB#
126	SIN2	IN <sub>T0</sub>	VDD3	SINB
127	DSR2#	IN <sub>T0</sub>	VDD3	DSRB#
128	CTS2#	IN <sub>T0</sub>	VDD3	CTSB#

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		<b>MICRO-STAR INT'L CO.,LTD</b>	
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Name	Type	Tolerance	Power Well	Native or GP	Patton Function
GPIO0	IO	3.3 V	Core	GPI	FRONT_USB_P24_DET#
GPIO1	IO	3.3 V	Core	GPI	RESTORE_PCH#
GPIO2	IOD	5 V	Core	Native	PIRQE#
GPIO3	IOD	5 V	Core	Native	PIRQ_F#
GPIO4	IOD	5 V	Core	Native	PIRQ_G#
GPIO5	IOD	5 V	Core	Native	PIRQ_H#
GPIO6	IO	3.3 V	Core	GPI	IO_SMI#
GPIO7	IO	3.3 V	Core	GPI	MXM_TH_ALERT#
GPIO8	IO	3.3 V	Suspend	GPI	BRD_ID2
GPIO9	IO	3.3 V	Suspend	Native	USB_OCP#_REAR
GPIO10	IO	3.3 V	Suspend	Native	USB_OCP#_LAN
GPIO11	IO	3.3 V	Suspend	GPO	PWR_COMA_CFG1
GPIO12	IO	3.3 V	Suspend	Native	LAN_DISABLE#
GPIO13	IO	3.3 V	Suspend	GPI	INT_USB_P151_DET#
GPIO14	IO	3.3 V	Suspend	Native	OC7#
GPIO15	IO	3.3 V	Suspend	GPO	Reserved
GPIO16	IO	3.3 V	Core	GPI	HOOD_SW_DET#
GPIO17	IO	3.3 V	Core	GPO	Reserved
GPIO18 (Mobile Only)	IO	3.3 V	Core	Native	N/A
GPIO19	IO	3.3 V	Core	GPI	Reserved
GPIO20	IO	3.3 V	Core	Native	PCIECLKRQ2#
GPIO21	IO	3.3 V	Core	GPI	FRONT_AUD_DET#
GPIO22	IO	3.3 V	Core	GPI	INT_USB_P150_DET#
GPIO23	IO	3.3 V	Core	Native	LDRQ1#
GPIO24	IO	3.3 V	Suspend	GPI	BRD_REV1
GPIO25 (Mobile Only)	IO	3.3 V	Suspend	Native	N/A
GPIO26 (Mobile Only)	IO	3.3 V	Suspend	Native	N/A
GPIO27	IO	3.3 V	Deep Sleep	GPI	DSW_WOL_WAKE
GPIO28	IO	3.3 V	Suspend	GPO	RSTBTN_EN#
GPIO29	IO	3.3 V	Suspend	Native	SLP_LAN#
GPIO30	IO	3.3 V	Deep Sleep	Native	SUS_WARN#
GPIO31	IO	3.3 V	Deep Sleep	GPI	Reserved
GPIO32 (not available in mobile)	IO	3.3 V	Core	GPI	STD_PS_DET#
GPIO33	IO	3.3 V	Core	GPI	PRNTR_DET#
GPIO34	IO	3.3 V	Core	GPI	HOOD_LOCK_DET
GPIO35	IO	3.3 V	Core	GPI	BRD_REV0

GPIO36	IO	3.3 V	Core	GPO	PWR_COMA_CFG0
GPIO37	IO	3.3 V	Core	GPO	PWR_COMB_CFG0
GPIO38	IO	3.3 V	Core	GPI	CHASSIS_ID0
GPIO39	IO	3.3 V	Core	GPI	BRD_ID1
GPIO40	IO	3.3 V	Suspend	Native	OC1#
GPIO41	IO	3.3 V	Suspend	Native	OC2#
GPIO42	IO	3.3 V	Suspend	Native	USB_OCP#_FRONT
GPIO43	IO	3.3 V	Suspend	GPI	PASSWORD_EN
GPIO44	IO	3.3 V	Suspend	GPI	DWR_STATUS
GPIO45	IO	3.3 V	Suspend	GPI	PCIE_RISER#
GPIO46	IO	3.3 V	Suspend	GPI	PCI_RISER#
GPIO47 (Mobile Only)	IO	3.3 V	Suspend	Native	N/A
GPIO48	IO	3.3 V	Core	GPI	CHASSIS_ID1
GPIO49	IO	3.3 V	Core	GPI	BRD_ID0
GPIO50	IO	5.0 V	Core	Native	REQ1#
GPIO51	IO	3.3 V	Core	Native	GNT1#
GPIO52	IO	5.0 V	Core	Native	REQ2#
GPIO53	IO	3.3 V	Core	Native	GNT2#
GPIO54	IO	5.0 V	Core	GPI	BOOT_BLK_EN#
GPIO55	IO	3.3 V	Core	GPO	LPC_DISABLE#
GPIO56 (Mobile Only)	IO	3.3 V	Suspend	Native	N/A
GPIO57	IO	3.3 V	Suspend	GPI	PWR_SER_DET#
GPIO58	IO	3.3 V	Suspend	Native	SML1CLK
GPIO59	IO	3.3 V	Suspend	Native	USB_OCP#_MEDIA
GPIO60	IO	3.3 V	Suspend	GPO	MXM_PWR_LEVEL
GPIO61	IO	3.3 V	Suspend	Native	SUS_STAT#
GPIO62	IO	3.3 V	Suspend	Native	SUSCLK
GPIO63	IO	3.3 V	Suspend	Native	SLP_S5#
GPIO64	IO	3.3 V	Core	Native	CLKOUTFLEX0
GPIO65	IO	3.3 V	Core	Native	CLKOUTFLEX1
GPIO66	IO	3.3 V	Core	Native	CLKOUTFLEX2
GPIO67	IO	3.3 V	Core	Native	CLKOUTFLEX3
GPIO68	IO	3.3 V	Core	GPI	FRONT_USB_P25_DET#
GPIO69	IO	3.3 V	Core	GPI	COMM_B_DET#
GPIO70	IO	3.3 V	Core	GPI	BOOT_BLK_REC#
GPIO71	IO	3.3 V	Core	GPO	GFX_RST#
GPIO72	IO	3.3 V	Suspend	Native (Mobile Only)	BATLOW#
GPIO73 (Mobile Only)	IO	3.3 V	Suspend	Native	N/A
GPIO74	IO	3.3 V	Suspend	GPO	PWR_COMB_CFG1
GPIO75	IO	3.3 V	Suspend	Native	SML1DATA

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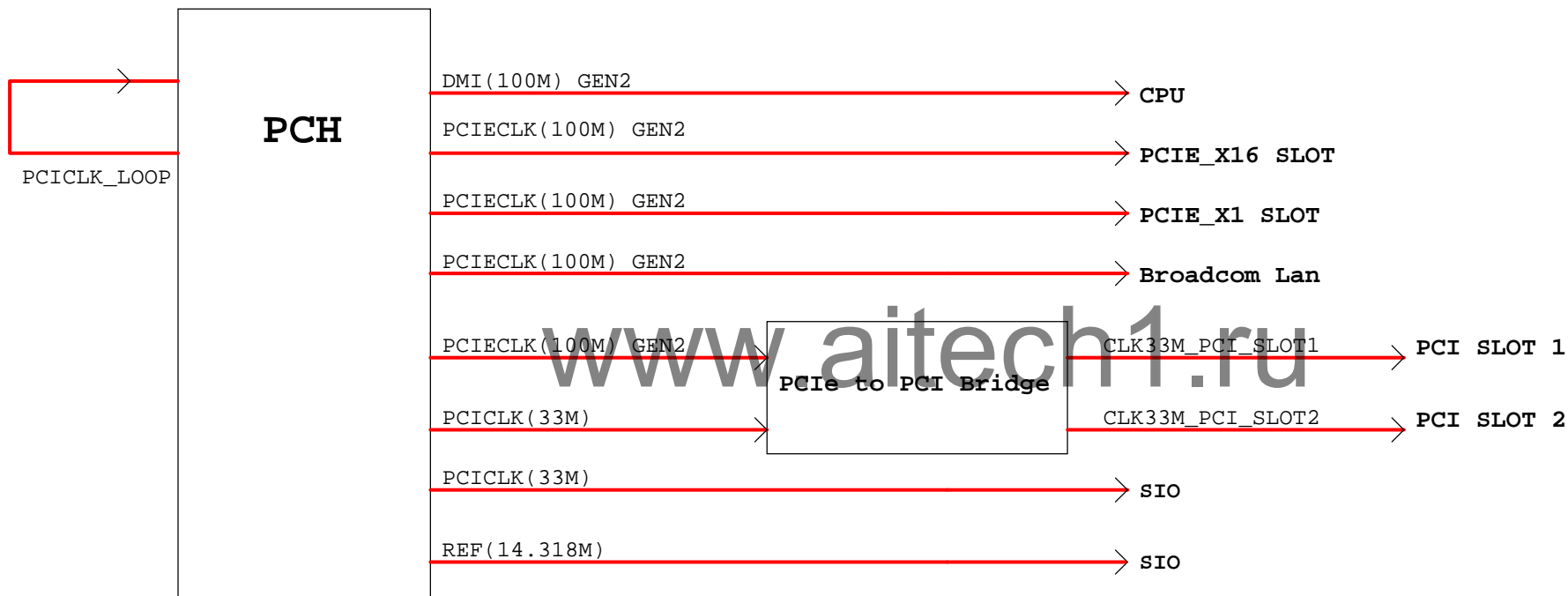
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Document Description  
PCH GPIO Table

Rev  
X2

Date:

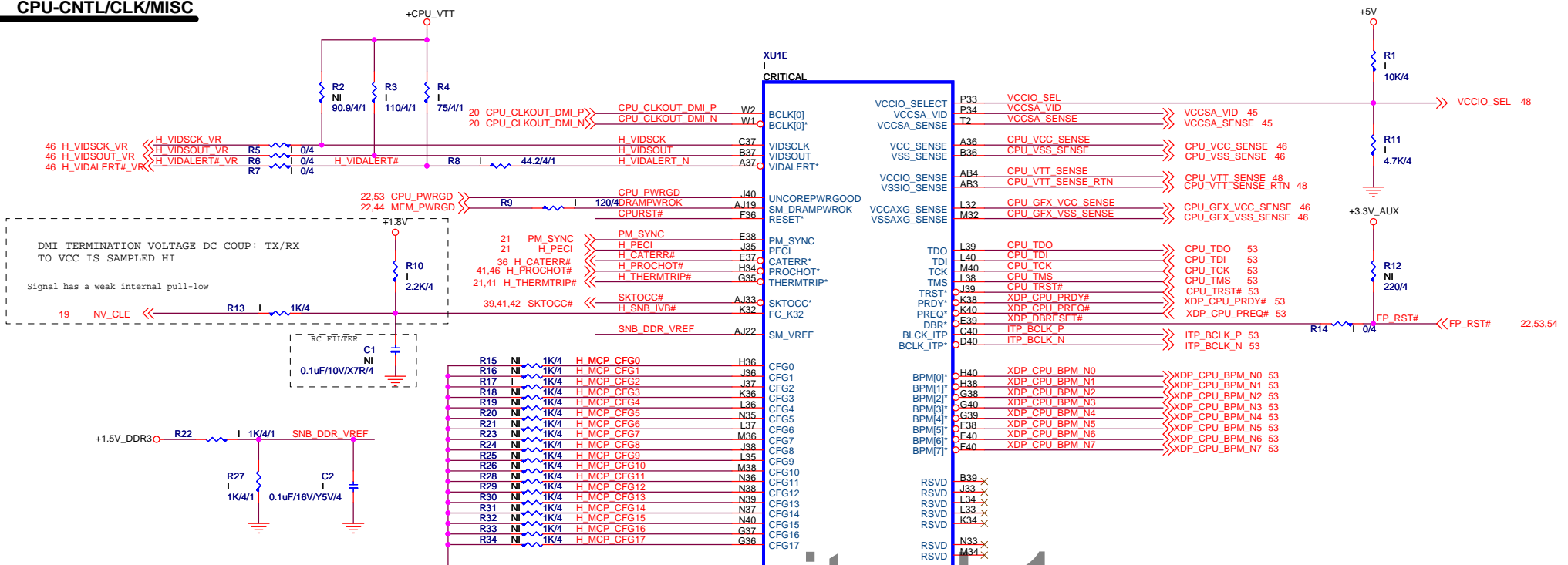
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# CPU-NTL/CLK/MISC



\* CFG[6:5] BIFURCATION: 11=DEAULT X16, 10=2X8, 01=RESERVED, 00=X8,X4,X4 \*

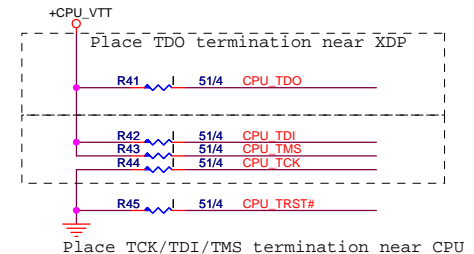
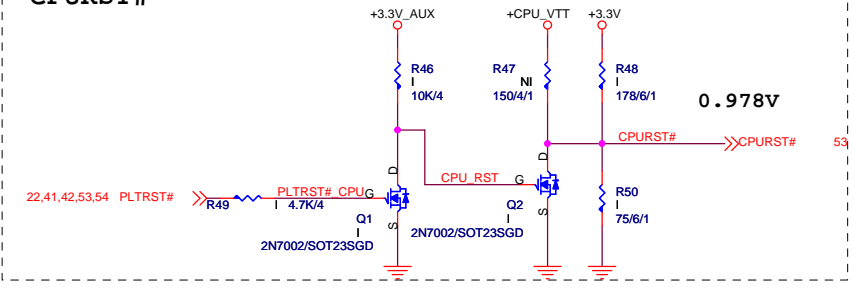
CFG	H	L	DESCRIPTION
0	REVERSED	REVERSED	REVERSED
1	REVERSED	REVERSED	REVERSED
2	NORM	REVERS	PEG LANE REVERSAL[0],X16
3	REVERSED	REVERSED	REVERSED
4	REVERSED	REVERSED	REVERSED
5	*	*	PCIE BIFURCATION
6	*	*	PCIE BIFURCATION
7	REVERSED	REVERSED	REVERSED
8	REVERSED	REVERSED	REVERSED
9	REVERSED	REVERSED	REVERSED
10	REVERSED	REVERSED	REVERSED
11	REVERSED	REVERSED	REVERSED
12	REVERSED	REVERSED	REVERSED
13	REVERSED	REVERSED	REVERSED
14	REVERSED	REVERSED	REVERSED
15	REVERSED	REVERSED	REVERSED

CFG 3,4,5,6,7,8,9 HAVE INTERNAL PULL-UPS

## PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

## CPURST#

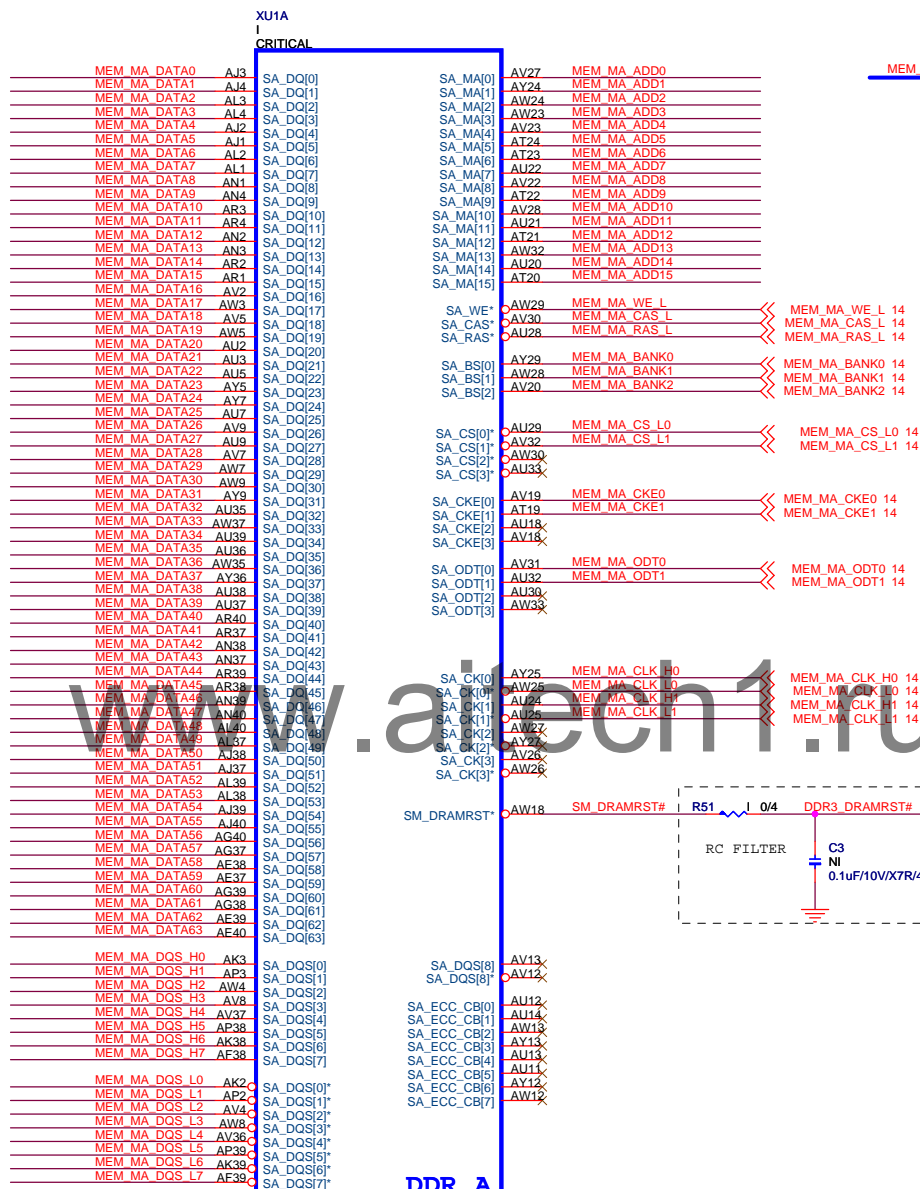


Release Date : Wednesday, November 23, 2011

**MICRO-STAR INT'L CO.,LTD**  
**HP SCH P/N: 675886-000 (MSI MS-7782)**  
 Size Custom Document Description  
**CPU-CLK/Control/MISC**  
 Date: Sheet 7 of 63

## CPU Memory CH-A

14 MEM\_MA\_DATA[63..0] &lt;&lt;&gt; MEM\_MA\_DATA[63..0]



Release Date : Wednesday, November 23, 2011



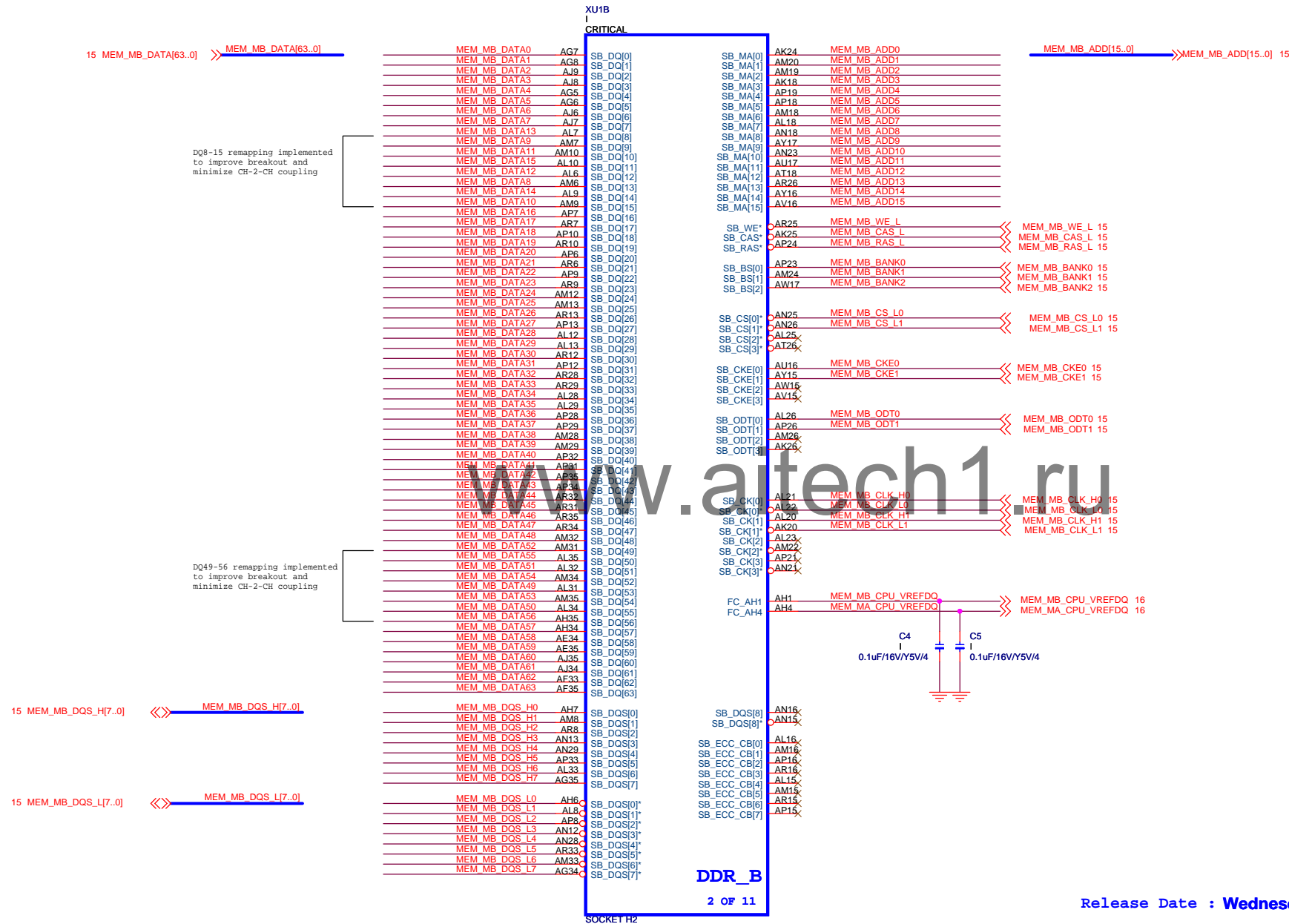
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	CPU-Memory-CHA	X2
Date:	Sheet 8 of 63	



## CPU Memory CH-B



DDR\_B

2 OF 11

Release Date : Wednesday, November 23, 2011

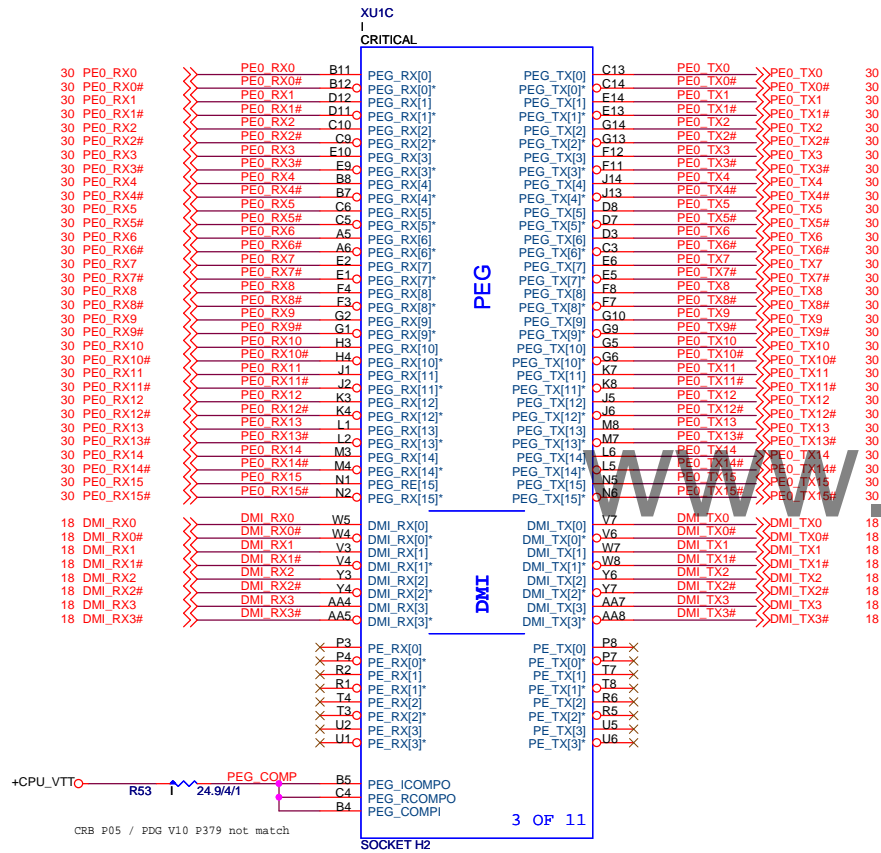


**MICRO-STAR INT'L CO.,LTD**

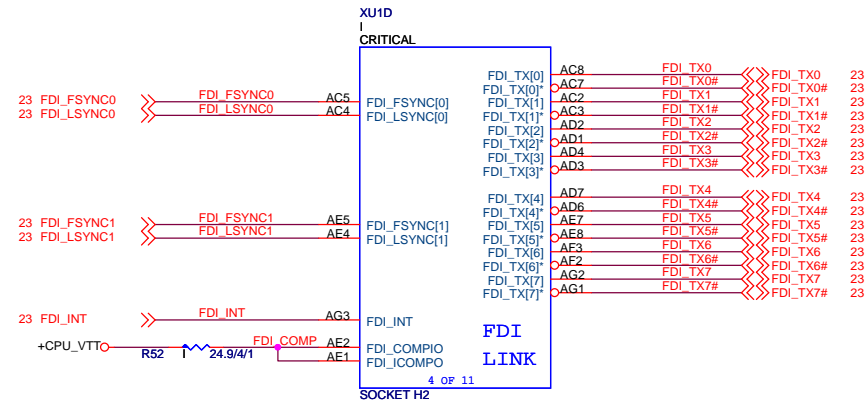
**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size Custom	Document Description <b>CPU-Memory-CHB</b>	Rev X2
Date:	Sheet 9 of 63	

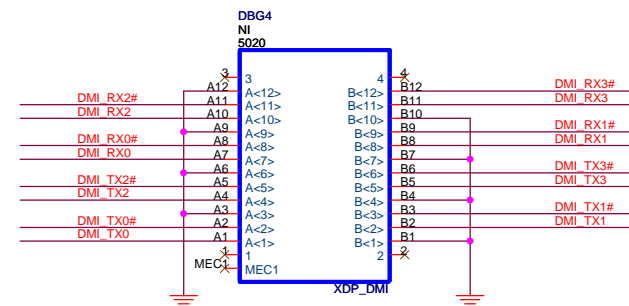
## CPU-PCIE / DMI



**CPU-FDI**



## XDP-DMI



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**MICRO-STAR INT'L CO.,LTD**

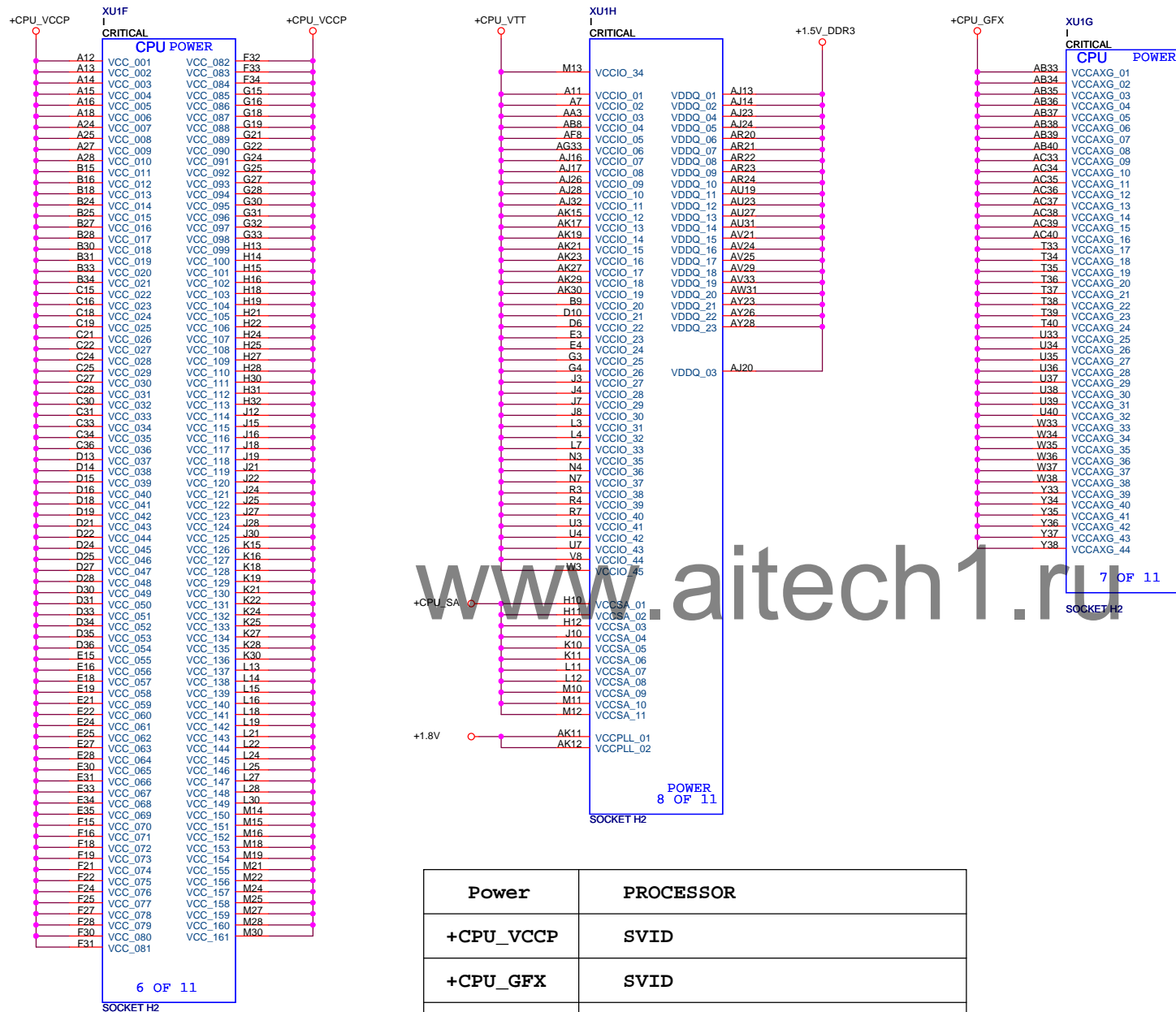
**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size	Document Description
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CPU-PCIE/DMI

Date:	Sheet 10 of 63
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# CPU-POWER



Power	PROCESSOR
+CPU_VCCP	SVID
+CPU_GFX	SVID
+CPU_VTT	1.05V/1.00V
+CPU_SA	0.96V/0.85V
+1.5V_DDR3	1.5V
+1.8V	1.8V

Release Date : Wednesday, November 23, 2011

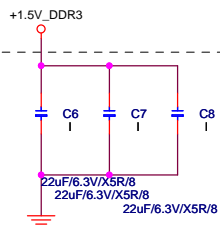
MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 675886-000 (MSI MS-7782)		
Size Custom	Document Description CPU-Power	Rev X2
Date:	Sheet 11 of 63	

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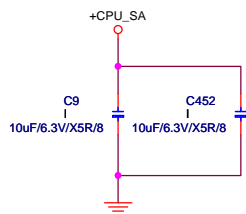


Size Custom	Document Description <b>CPU-GND</b>	Rev X2
Date:	Sheet 12 of 63	

### +1.5V\_DDR3-Decoupling

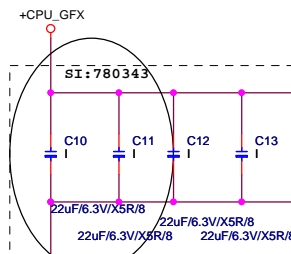


CPU SOCKET CAVITY CAPS 22uF X3

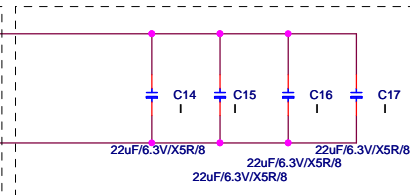


BOTTOM SIDE 22uF X 2

### +CPU\_GFX Decoupling

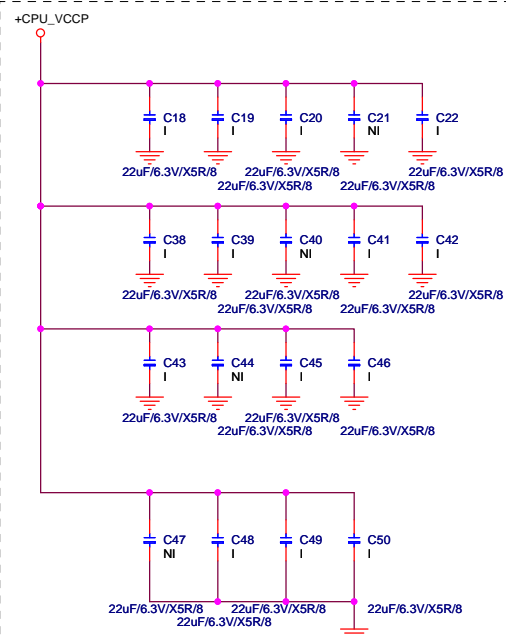


BOTTOM SIDE 22uF X 4



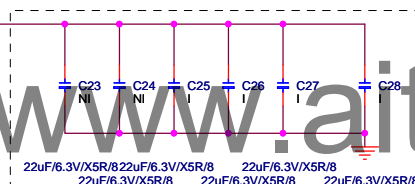
CPU SOCKET CAVITY CAPS 22uF X 4

### +CPU\_VCCP-Decoupling



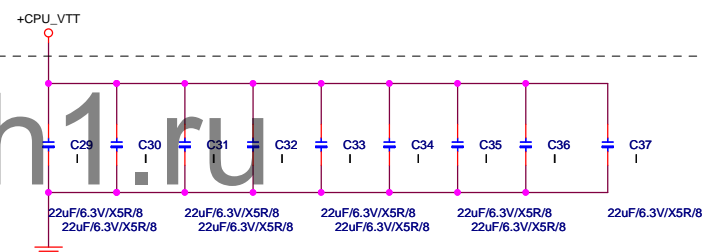
INSIDE CPU SOCKET CAVITY 22uF X 14

+CPU\_VCCP

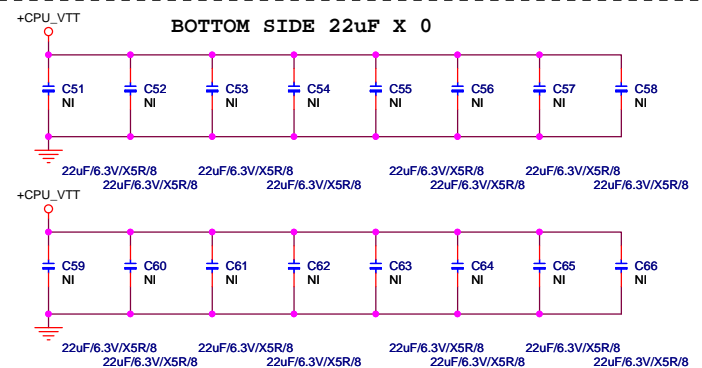


BOTTOM SIDE 22uF X 4

### +CPU\_VTT Decoupling



CPU SOCKET CAVITY CAPS 22uF X 9



BOTTOM SIDE 22uF X 0

Release Date : Wednesday, November 23, 2011



MICRO-STAR INT'L CO.,LTD

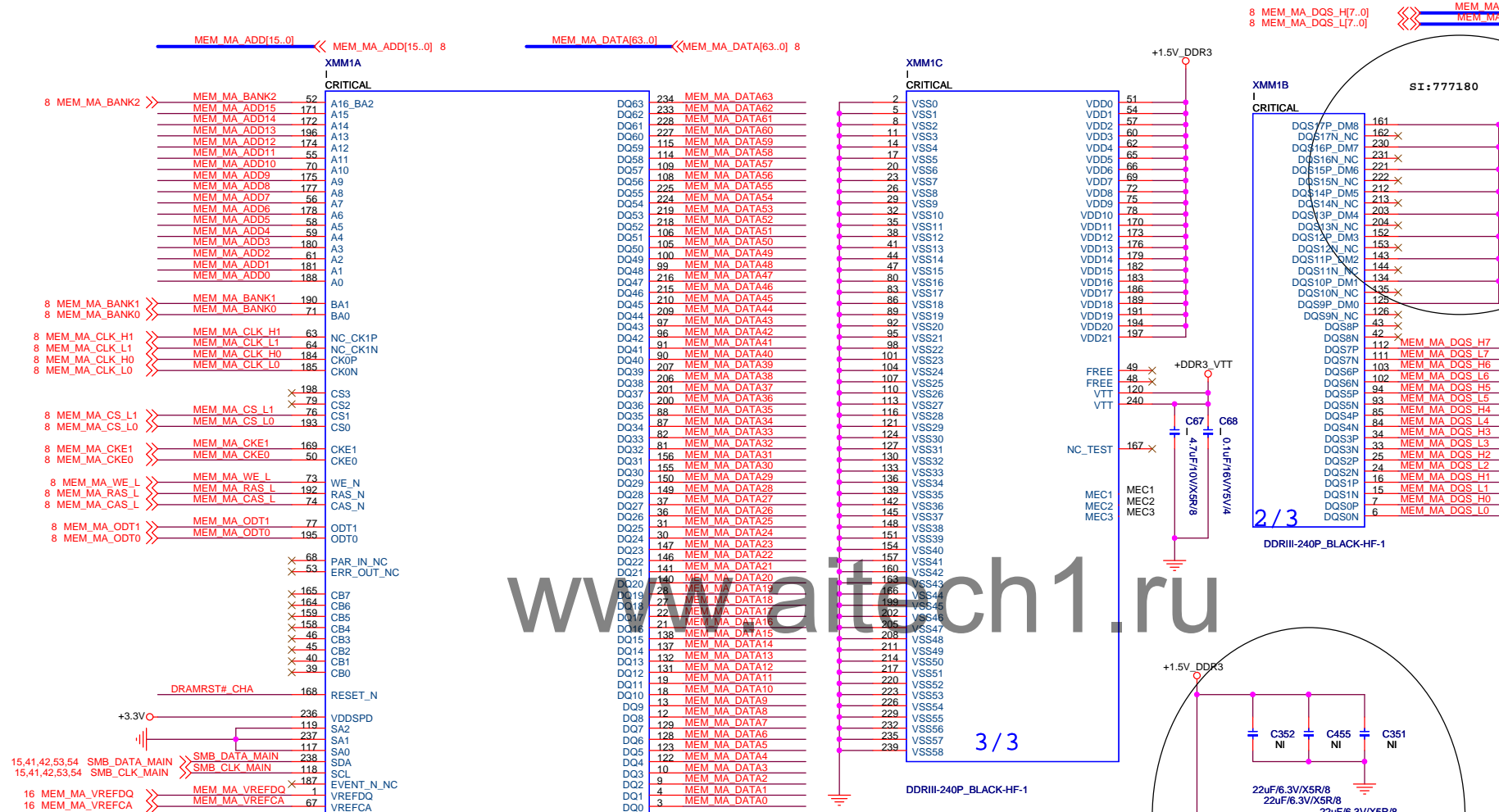
HP SCH P/N: 675886-000 (MSI MS-7782)

Document Description  
CPU-Decoupling

Rev  
X2

Date: Sheet 13 of 63

# DDR3 CH-A DIMM1

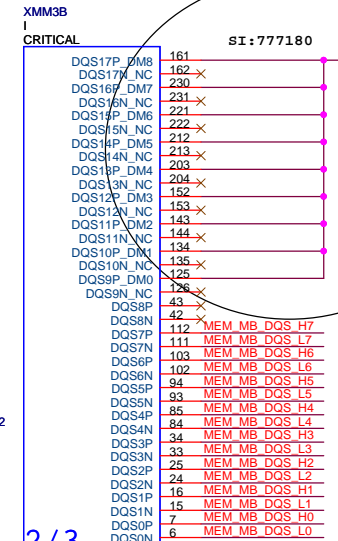


Release Date : Wednesday, November 23, 2011


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>		
Size Custom	Document Description <b>DDR DIMM 1</b>	Rev X2
Date:	Sheet 14 of 63	



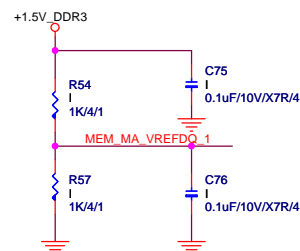
MEM\_MB\_DATA[63..0] 9



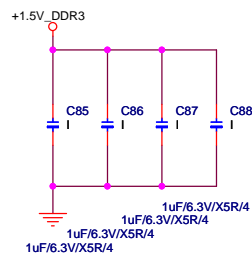
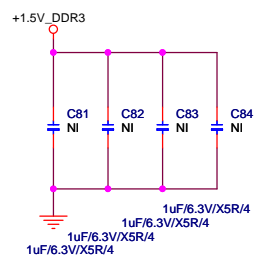
**Black COLOR**

	<b>MICRO-STAR INT'L CO.,LTD</b>				
	<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>				
	Size Custom	Document Description <b>DDR DIMM 2</b>			Rev X2
	Date:		Sheet	15	of 63

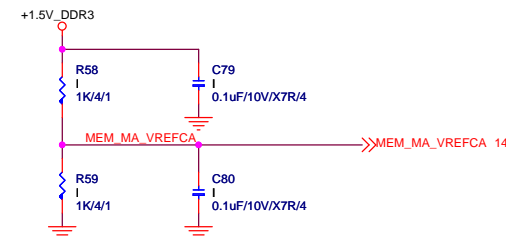
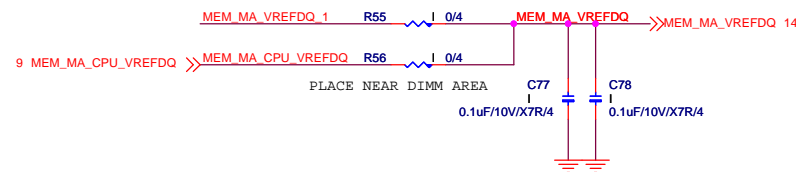
# CHA



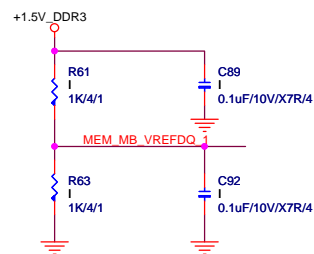
PLACE RESISTORS CLOSE TO CH\_A DIMMS ON MEM\_MA\_VREFDQ



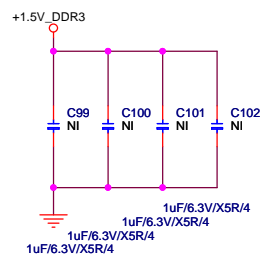
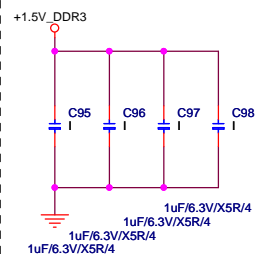
FOR XMM1



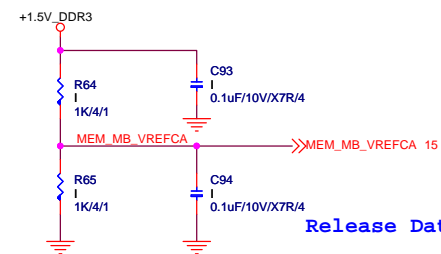
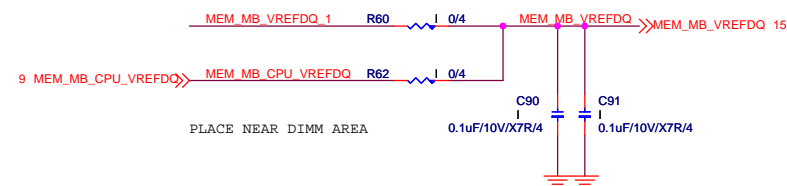
# CHB



PLACE RESISTORS CLOSE TO CH\_B DIMMS ON MEM\_MB\_VREFDQ



FOR XMM3



Release Date : Wednesday, November 23, 2011



MICRO-STAR INT'L CO.,LTD


HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	CHA VREF OPTION	X2
Date:	Sheet 16 of 63	



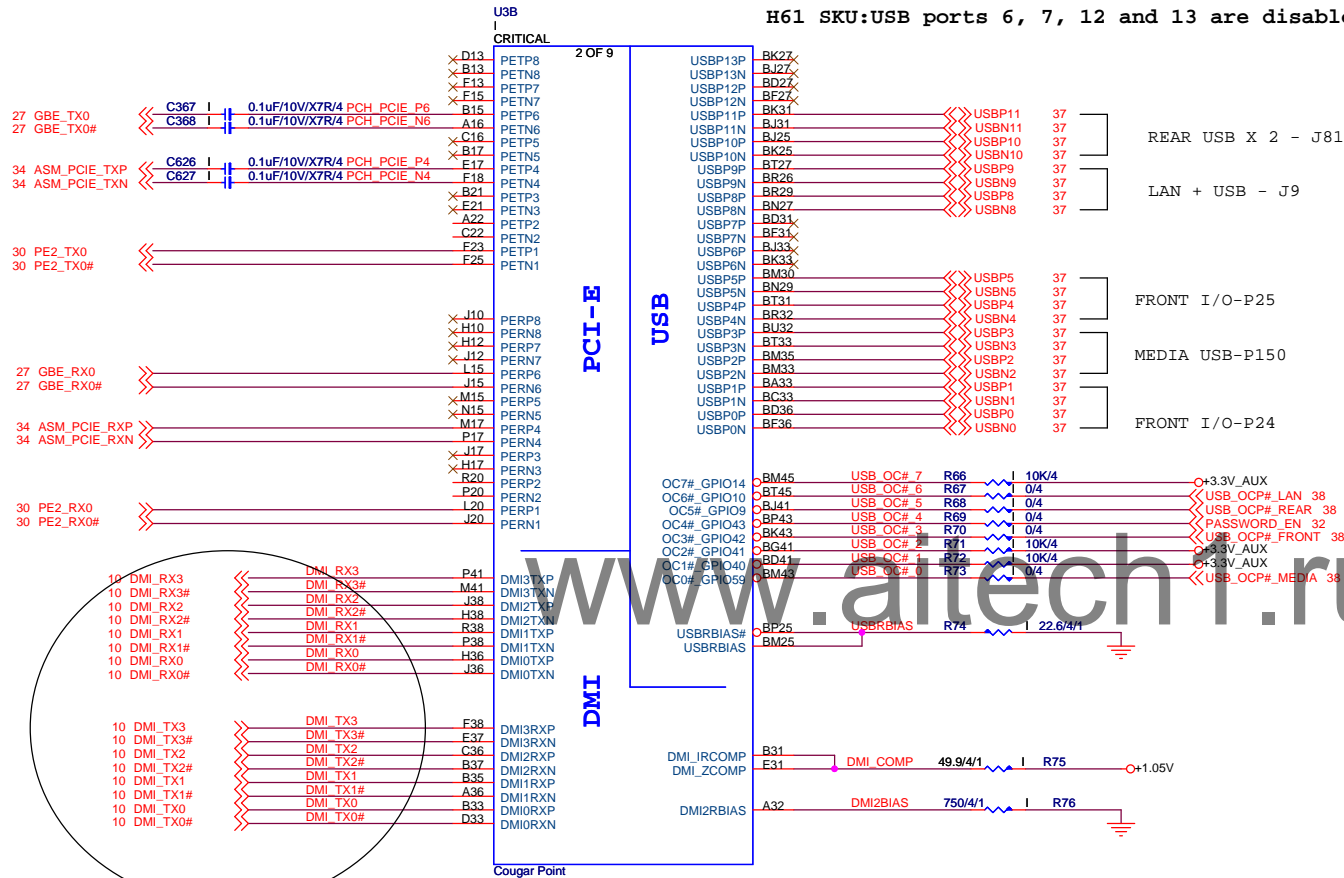
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Release Date : Wednesday, November 23, 2011

		MICRO-STAR INT'L CO.,LTD	
		HP SCH P/N: 675886-000 (MSI MS-7782)	
Size Custom	Document Description	CHB VREF OPTION	Rev X2
Date:	Sheet 17 of 63		

# PCH PCIE/DMI/USB

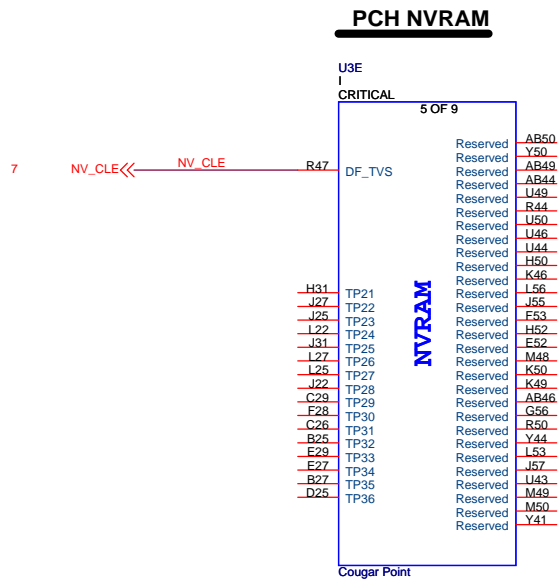
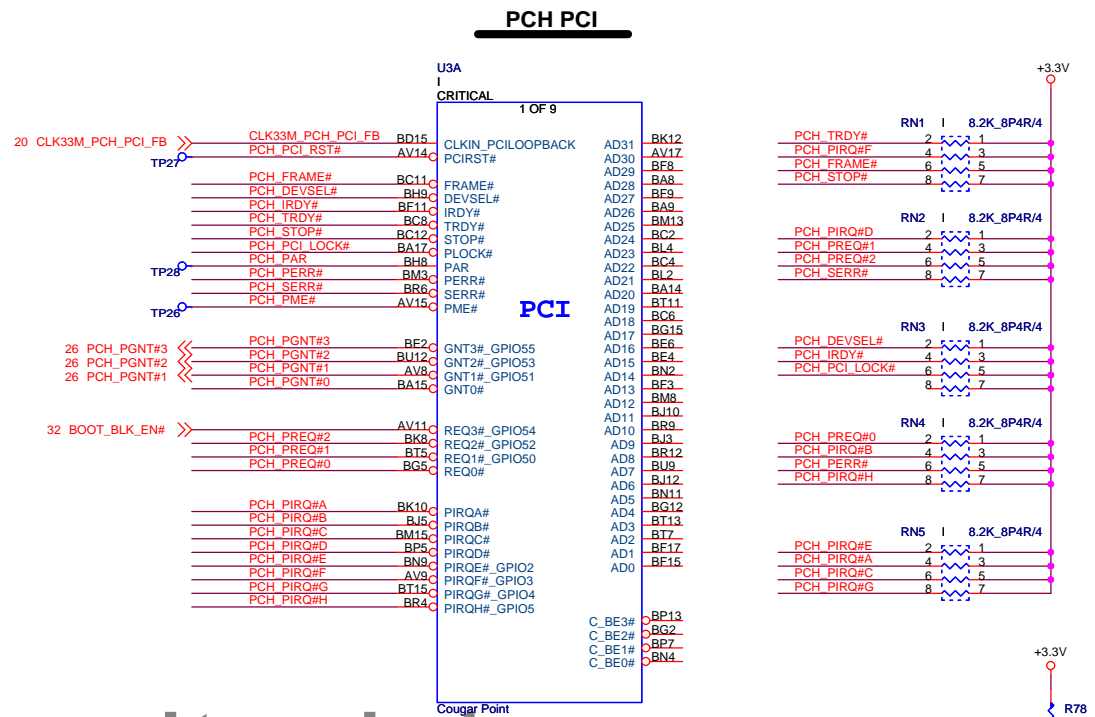
H61 SKU:PCie ports 7 and 8 are disabled.  
H61 SKU:USB ports 6, 7, 12 and 13 are disabled.



USB OC# 7	R219	PROTO 33/4	PCH_XDP 7	PCH_XDP 7	54
USB OC# 6	R352	PROTO 33/4	PCH_XDP 6	PCH_XDP 6	54
USB OC# 5	R442	PROTO 33/4	PCH_XDP 5	PCH_XDP 5	54
USB OC# 4	R444	PROTO 33/4	PCH_XDP 4	PCH_XDP 4	54
USB OC# 3	R457	PROTO 33/4	PCH_XDP 3	PCH_XDP 3	54
USB OC# 2	R791	PROTO 33/4	PCH_XDP 2	PCH_XDP 2	54
USB OC# 1	R792	PROTO 33/4	PCH_XDP 1	PCH_XDP 1	54
USB OC# 0	R793	PROTO 33/4	PCH_XDP 0	PCH_XDP 0	54

Release Date : Wednesday, November 23, 2011

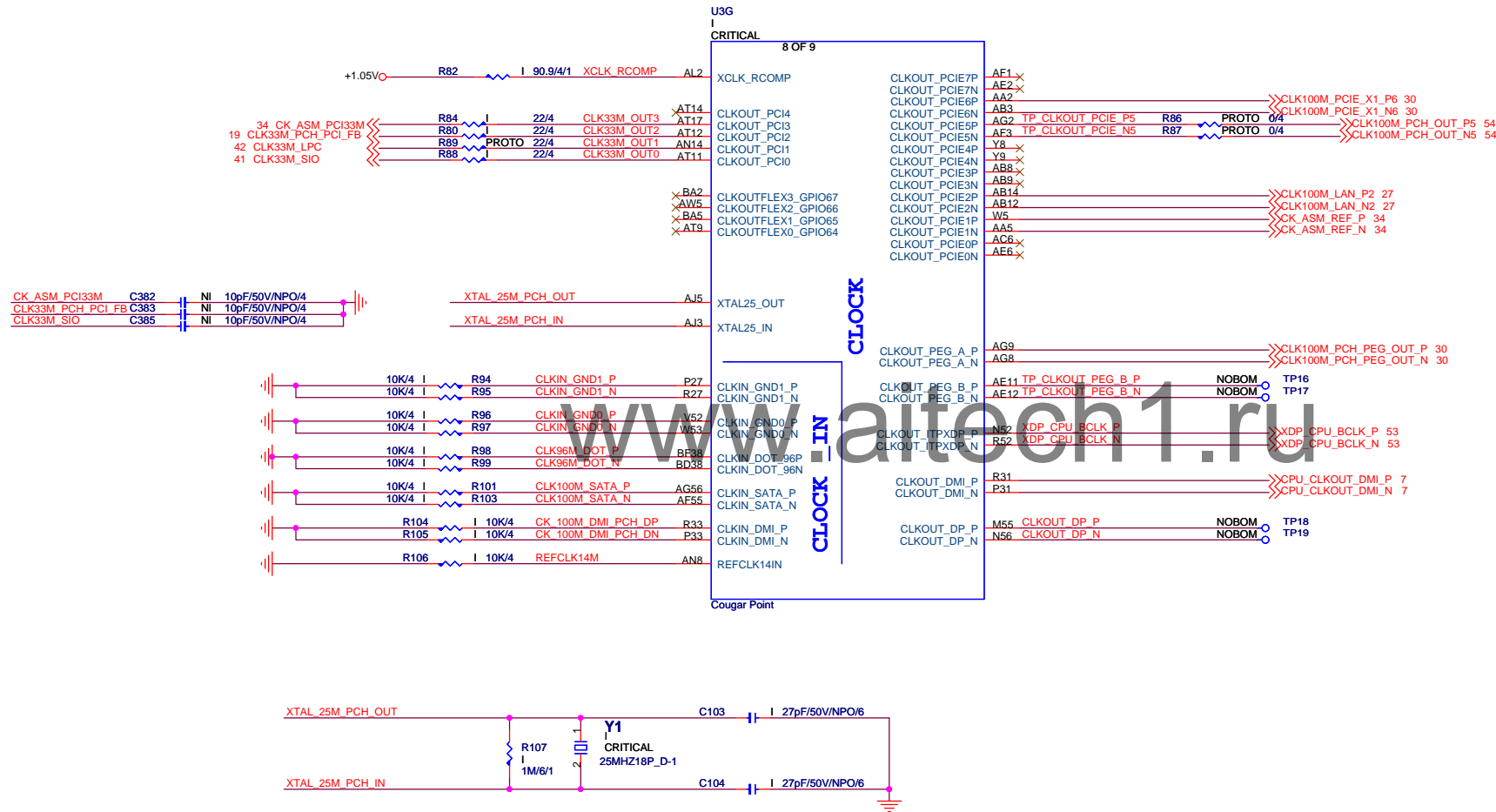
			<b>MICRO-STAR INT'L CO.,LTD</b>	
<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>				
Size	Document Description			Rev
Custom	<b>PCH PCIE/DMI/USB</b>			X2
Date:		Sheet	18	of 63



Release Date : Wednesday, November 23, 2011

		<b>MICRO-STAR INT'L CO.,LTD</b>	
		<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>	
Size Custom	Document Description <b>PCH PCI/NVRAM</b>	Rev X2	
Date:		Sheet	19 of 63

# PCH CLOCK



Release Date : Wednesday, November 23, 2011



MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

Size  
Custom

Document Description  
PCH CLOCK

Rev  
X2

Date:

Sheet 20 of 63

**PLACE SATA AC COUPLING CAPS CLOSE TO U3**

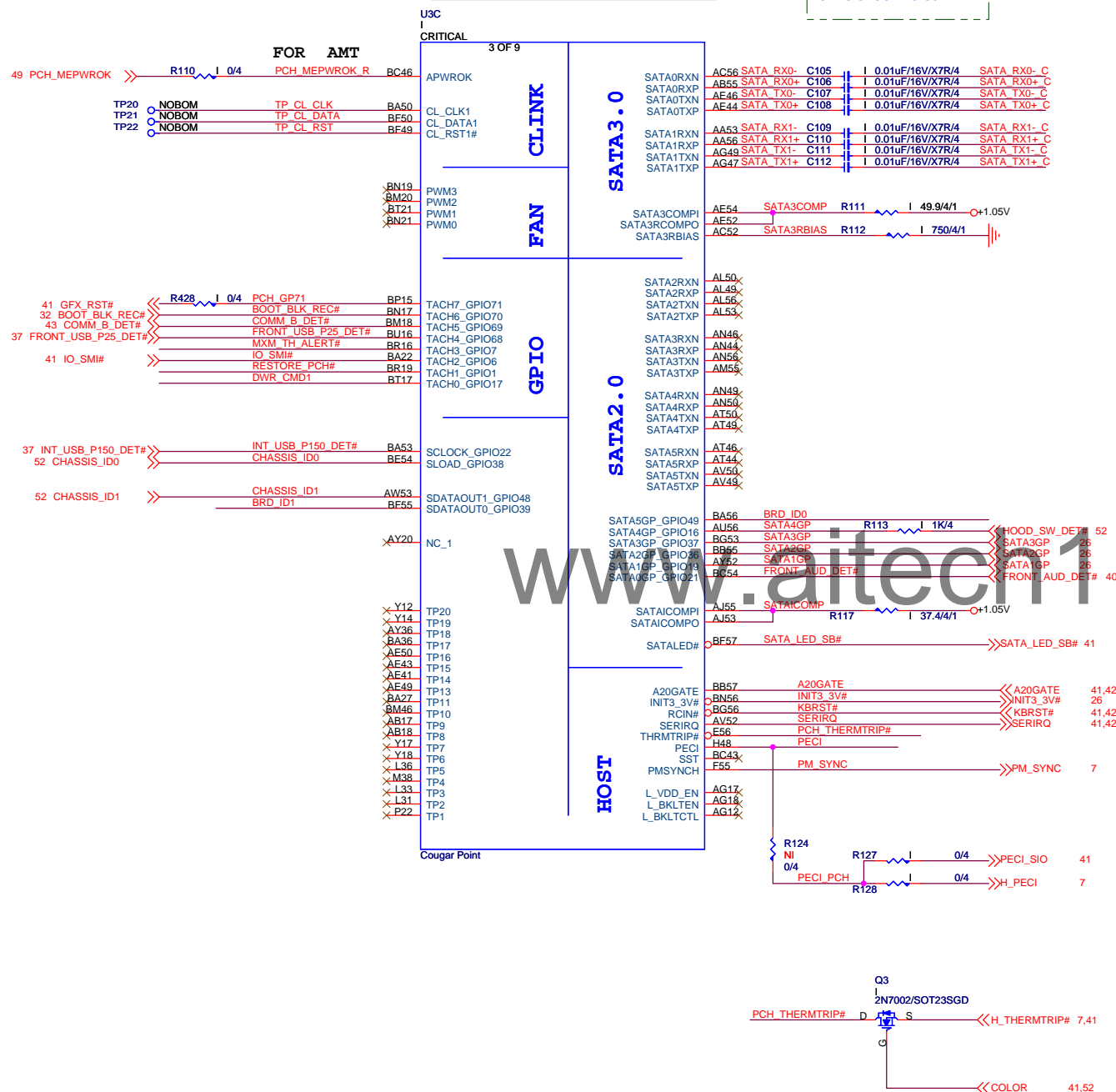
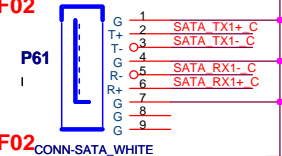


Diagram illustrating a 9-track tape configuration. The tape is labeled **P60** and **CONN-SATA DARKBLUE**. The tracks are numbered 1 through 9. Tracks 1, 2, 3, 4, 5, and 6 are highlighted with a blue box, indicating they are the active data tracks. Tracks 7, 8, and 9 are not highlighted. The labels for the tracks are: 1 G, 2 G+, 3 T-, 4 T, 5 G, 6 R+, 7 G, 8 G, 9 G.



22 BRD\_REV0 R129 NI 10K/4  
22 BRD\_REV1 R130 NI 10K/4

22 BRD\_REV0 R131 I 10K/4  
22 BRD\_REV1 R132 I 10K/4

BOARD REV[1:0]	Enterprise Desktop
00	All EVT
01	All DVT
10	PVT1
11	PVT2+
00	MVB, A
01	1st Major ECN
10	2 <sup>nd</sup> Major ECN
11	3 <sup>rd</sup> Major ECN

**ARD ID**

22 BRD\_ID2 >> 

BRD_ID0	R122	10K/4
BRD_ID1	R123	10K/4
BRD_ID2	R135	NI/10K/4

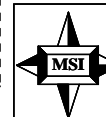
22 BRD\_ID2 >> 

BRD_ID0	R125	NI/10K/4
BRD_ID1	R126	NI/10K/4
BRD_ID2	R140	10K/4

+3.3V

Form Factor	Default	Commanders
Small Form Factor	011	

**Release Date : Wednesday, November 23, 2011**



**MICRO-STAR INT'L CO.,LTD**

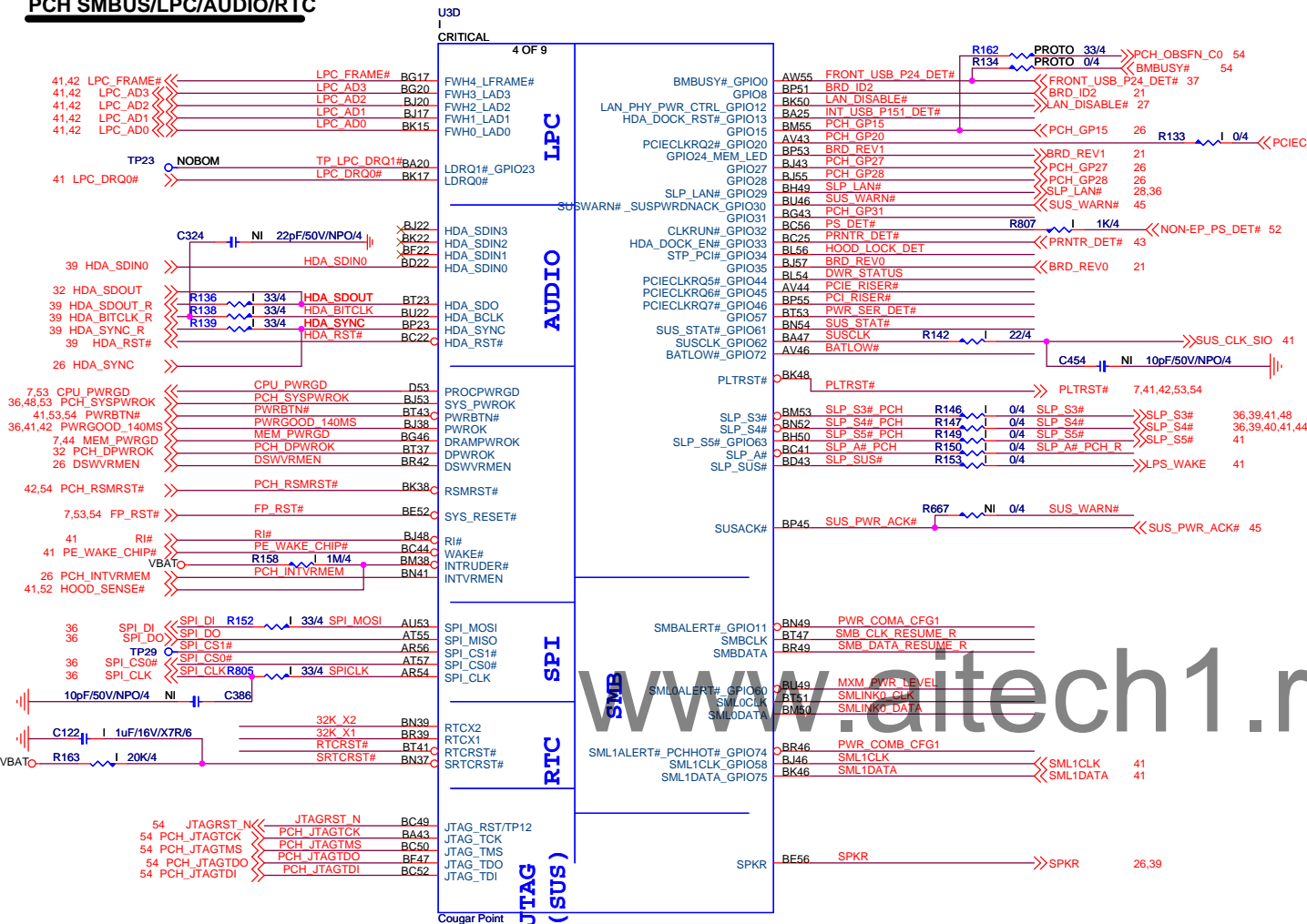
HP SCH P/N: 675886-000 (MSI MS-7782)

Size Custom	Document Description <b>PCH SATAII/HOST/FAN/GPIO</b>
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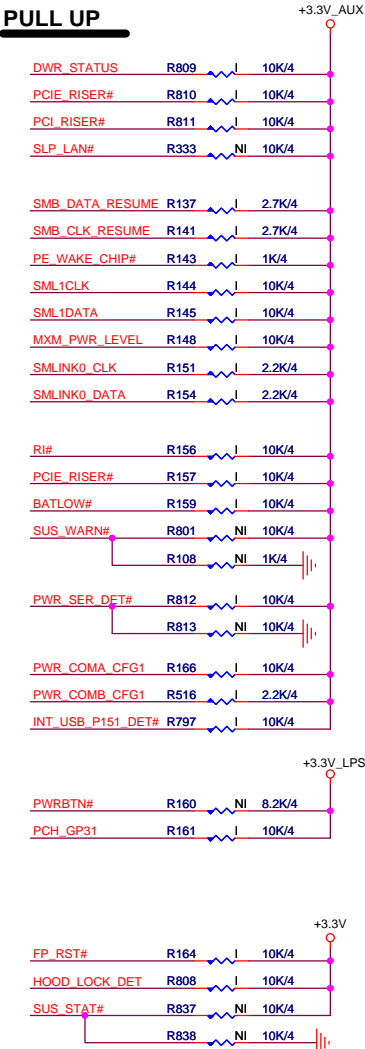
	Re
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Date:	Sheet 21 of 63
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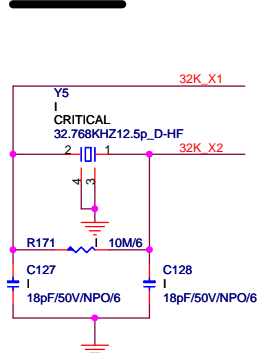
## PCH SMBUS/LPC/AUDIO/RTC



## PULL UP

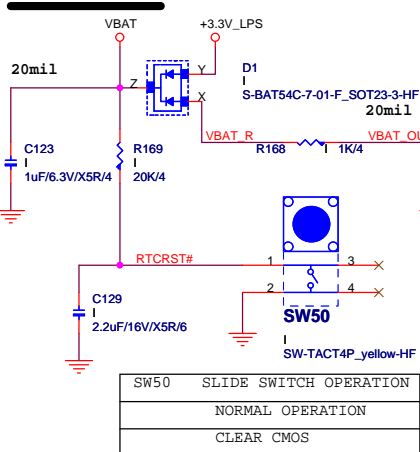


32.768KHZ

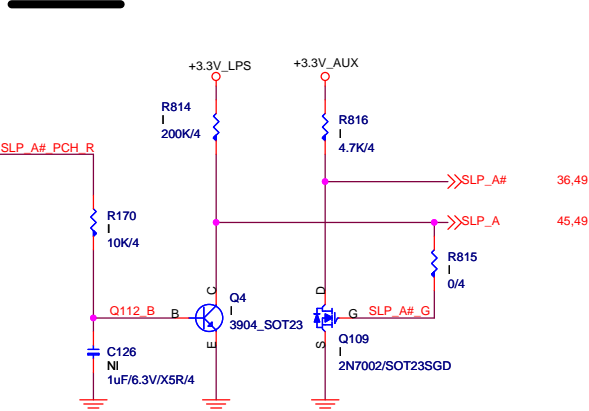


PLACE THESE COMPONENTS CLOSE TO U3, AND  
USE GROUND GUARD FOR 32K\_X1 AND 32K\_X2

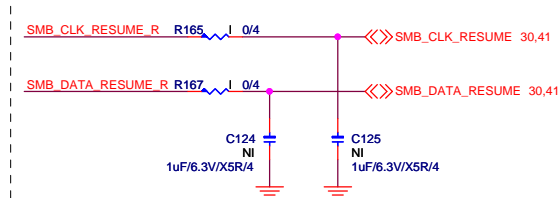
## CLEAR CMOS



SLP\_A



PLACE 0 OHM CLOSURE TO PCH



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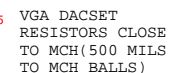
**MICRO-STAR INT'L CO.,LTD**

**HP SCH P/N: 675886-000 (MSI MS-7782)**

	Document Description
	<b>PCH SMBUS/LPC/AUDIO/RTC</b>

	Rev
	X

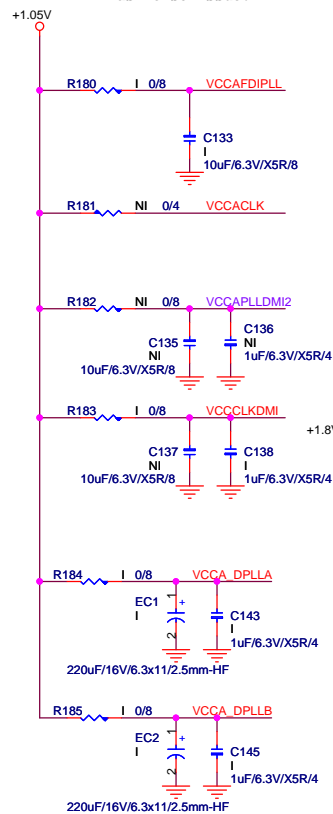
## Cougar Point



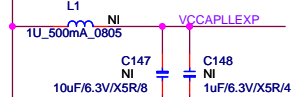
Size Custom	Document Description <b>PCH FDI/VGA/HDMI/DP/SDV</b>	Rev X2
Date:	Sheet 23 of 63	

# PCH POWER

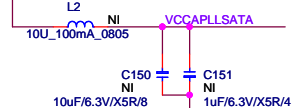
Change to 10UH if  
VCCA\_DPLLA/VCCA\_DPLLB  
has noise issue.



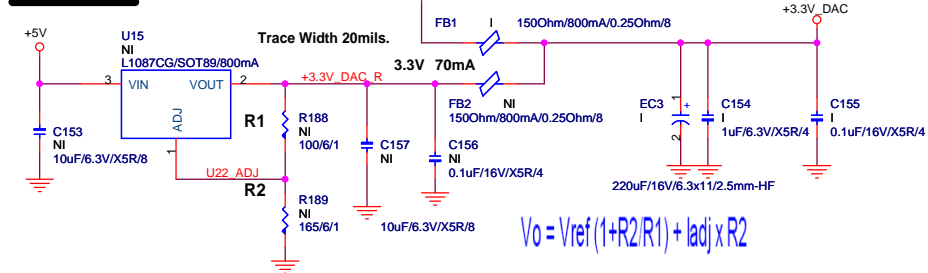
## DMI PLL FILTER



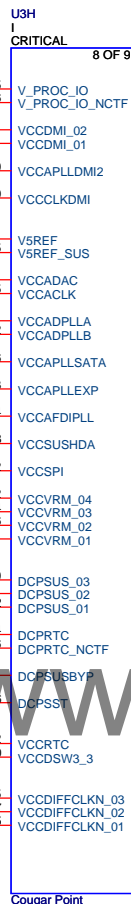
## SATA PLL FILTER



## +3.3V DAC



$$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} \times R_2$$

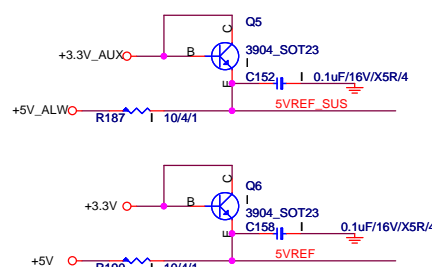


## POWER

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0.4 A

## 5VREF & 5VREF\_SUS Sequencing Circuit



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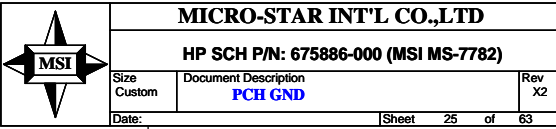


MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	PCH POWER	X2
Date:	Sheet 24 of 63	

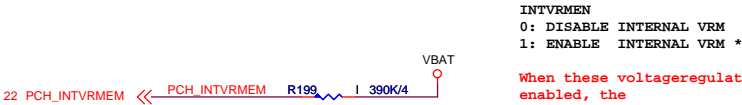
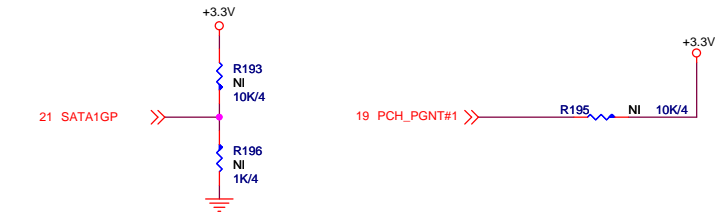






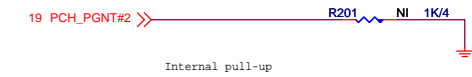
## REQUIRED STRAPS

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating

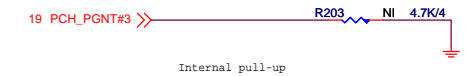


INTVRMEN  
0 : DISABLE INTERNAL VRM  
1 : ENABLE INTERNAL VRM \*

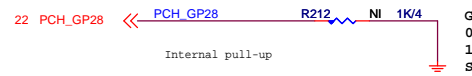
When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



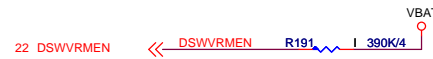
DMI AC/DC MODE  
0 : AC  
1 : DC \*



Topblock swap override when pull-low  
Signal has a weak internal pull-up



GPIO28  
0 : OD PLL VR disabled  
1 : OD PLL VR enabled \*  
Signal has a weak internal pull-up



DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

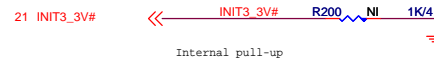
This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.



HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0 : 1.8V SUPPLY \*  
1 : 1.5V SUPPLY

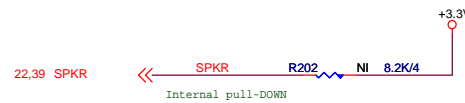


GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



INIT3\_3V#  
0 : ??????????????  
1 : ?????????????? \*

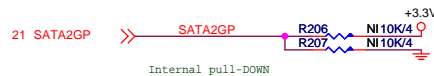
1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some events occur.  
0: Can not to reset the processor.



SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT



In Deep Sleep Power Well.  
If not used, require a weak pull-up (8.2k-10k) to VccDSW3\_3



Cougar point EDS PAGE:93 This signal should not be pull high



Cougar point EDS PAGE:93 This signal should not be pull high

Release Date : Wednesday, November 23, 2011



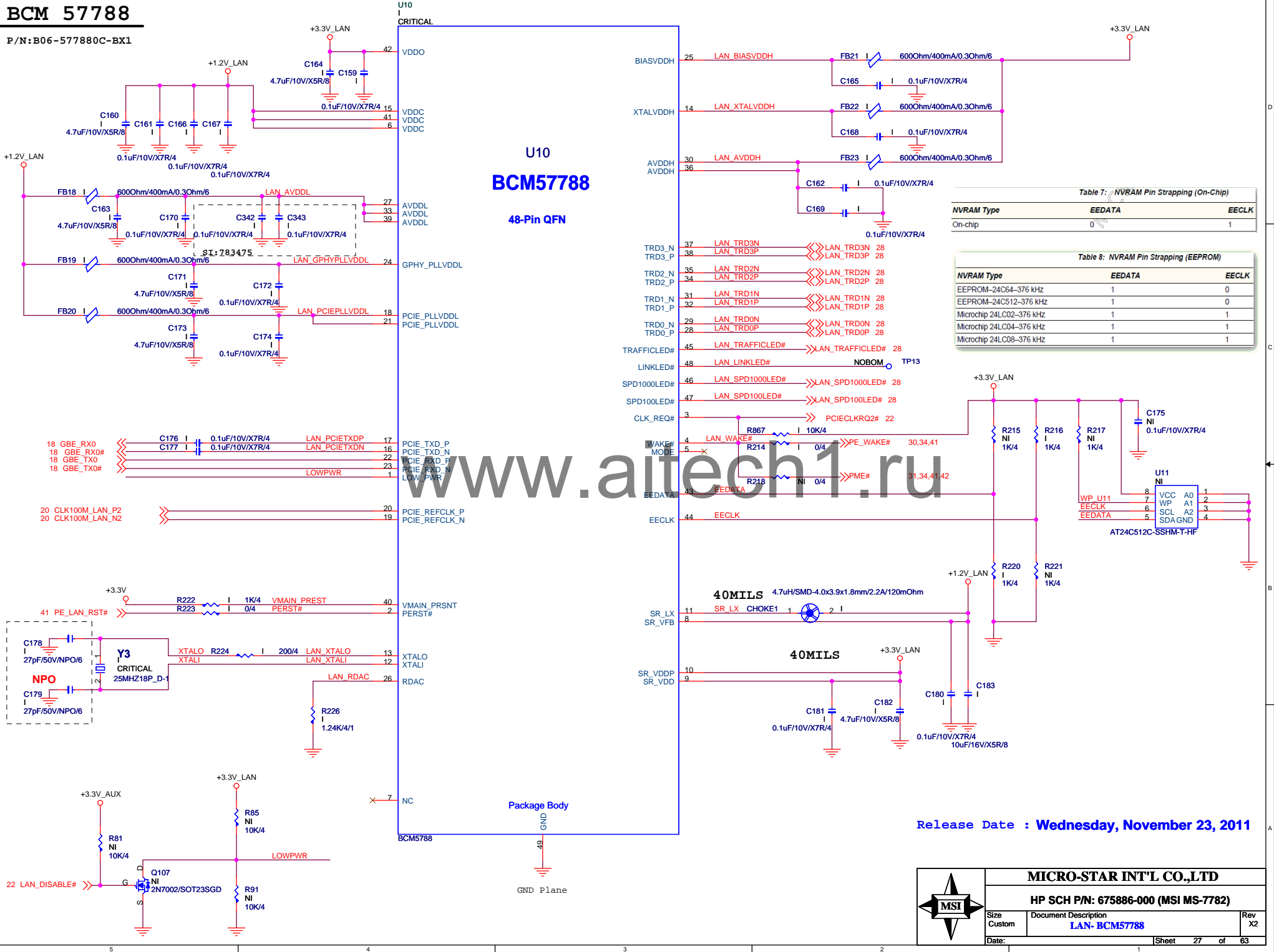
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

Size Custom	Document Description PCH STRAPS	Rev X2
Date:	Sheet 26 of 63	

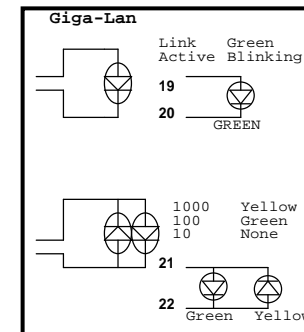
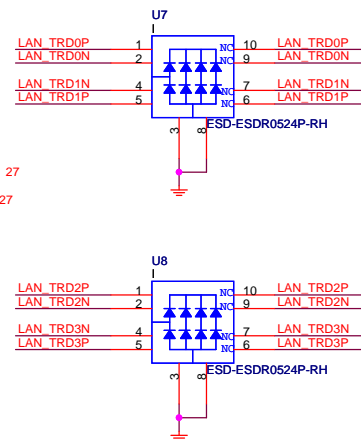
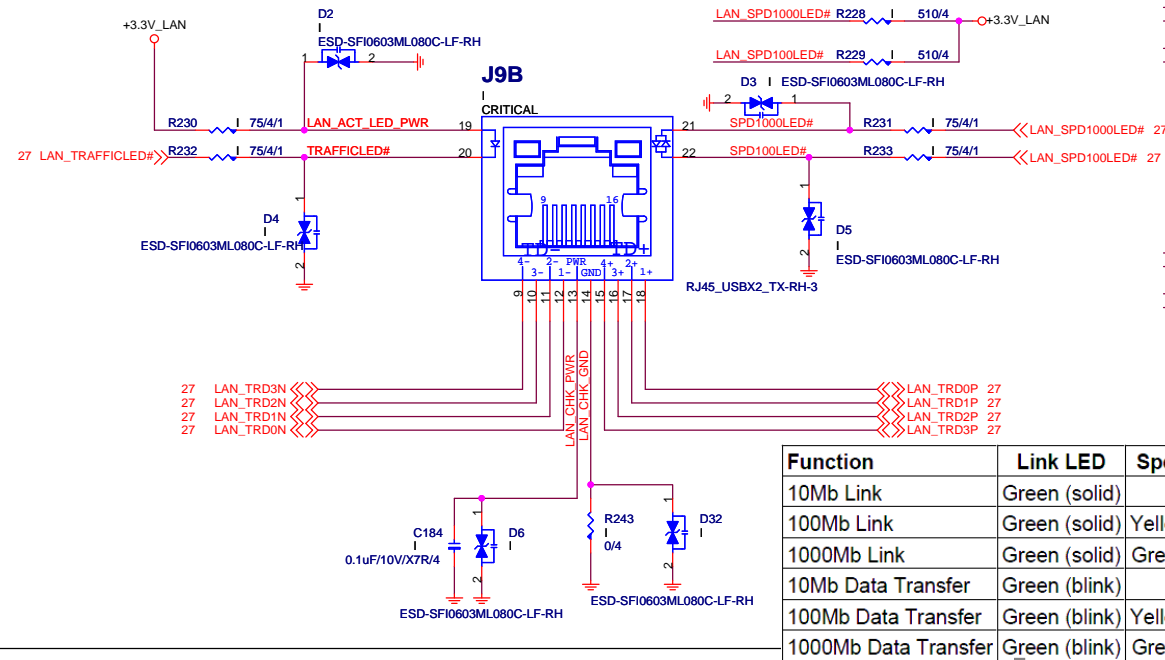
# BCM 57788

P/N: B06-577880C-BX1

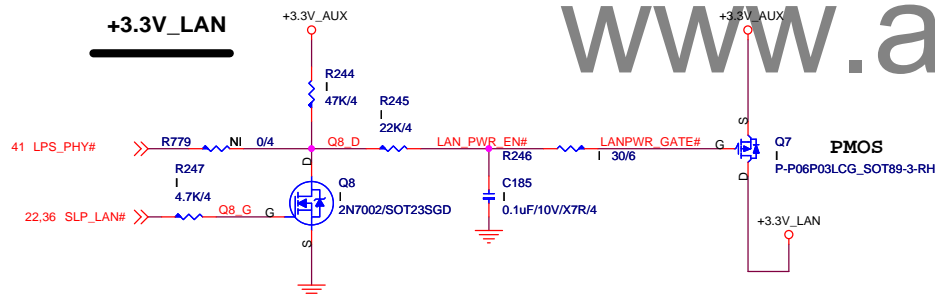
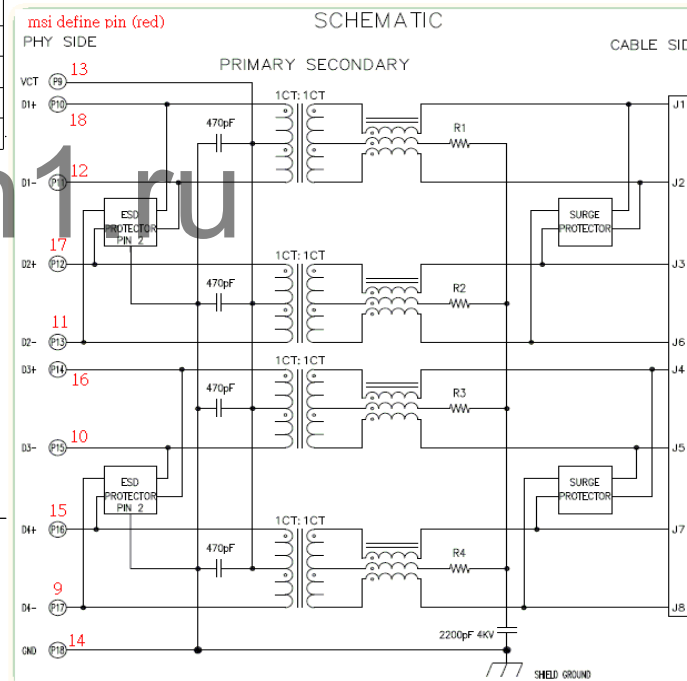
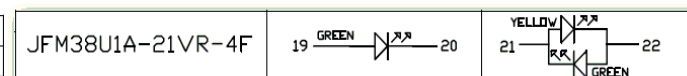


# LAN CONNECTOR


P/N:N58-22F1481-U30



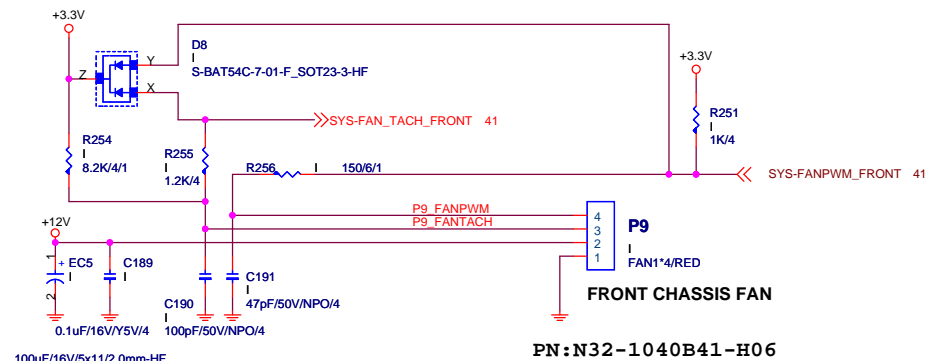
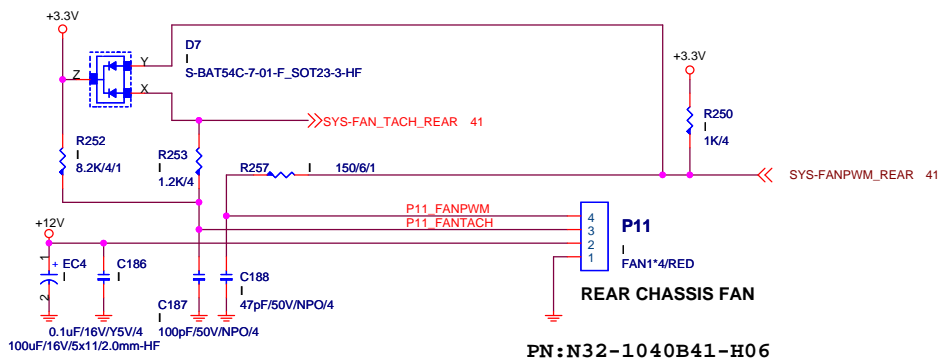
Function	Link LED	Speed LED
10Mb Link	Green (solid)	Off
100Mb Link	Green (solid)	Yellow (solid)
1000Mb Link	Green (solid)	Green (solid)
10Mb Data Transfer	Green (blink)	Off
100Mb Data Transfer	Green (blink)	Yellow (solid)
1000Mb Data Transfer	Green (blink)	Green (solid)



Release Date : Wednesday, November 23, 2011

			<b>MICRO-STAR INT'L CO.,LTD</b>	
<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>			<b>LAN POWER/CONN</b>	
Size	Document Description	Rev		X2
Custom				
Date:		Sheet	28	of 63

# FAN BLOCK



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Release Date : Wednesday, November 23, 2011

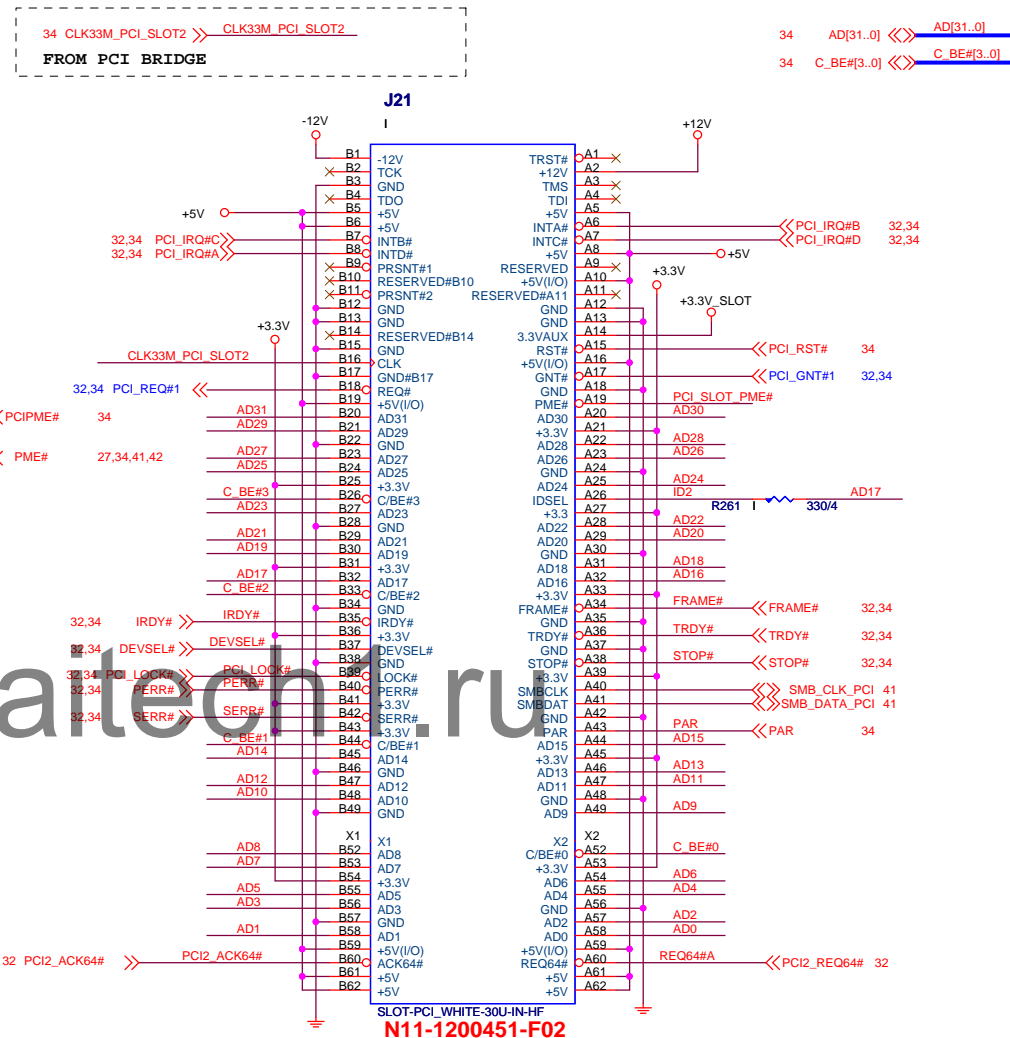


MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	FAN	X2
Date:	Sheet 29 of 63	




**PCI SLOT 1 (PCI VER: 2.3 COMPLY)**

```

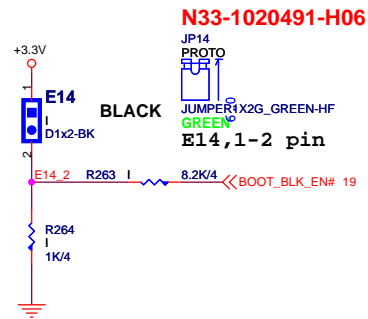
PCI_SLOT2
IDSEL = AD17
PCI_REQ#1
PCI_GNT#1
PCI_INTB#

```

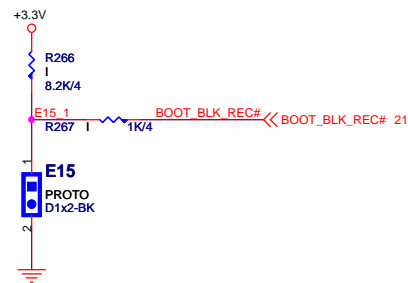
	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>		
	Size Custom	Document Description <b>PCI SLOT</b>	Revisions
Date:		Sheet 31 of 63	



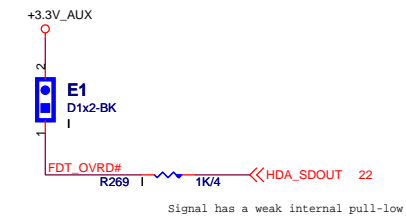
## BOOT BLOCK WRITE JUMPER



## BOOT BLOCK RECOVERY HEADER

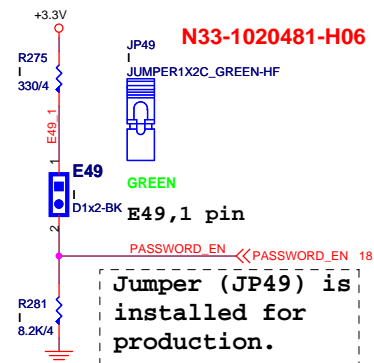


## FLASH DESCRIPTOR OVERRIDE

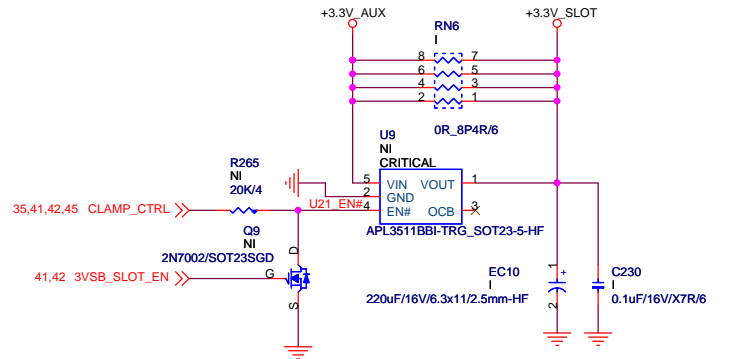


## N31-1020211-P05

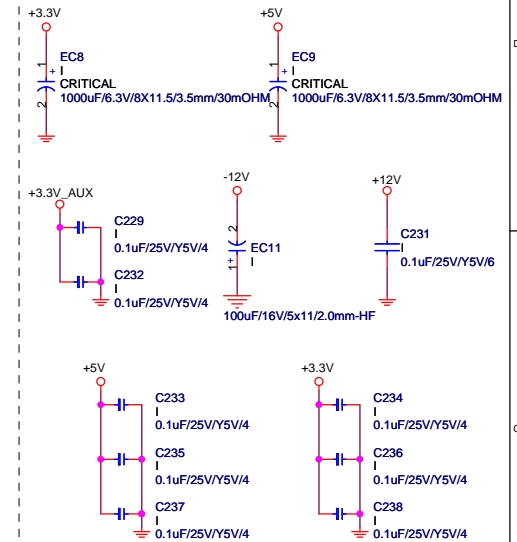
## PASSWORD JUMPER



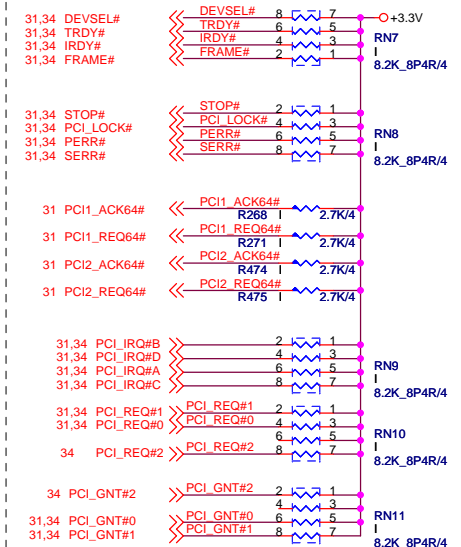
## +3.3V SLOT



## PCI SLOT DECOUPLING CAPACITORS



## PCI PULL-UP / DOWN RESISTORS



Release Date : Wednesday, November 23, 2011



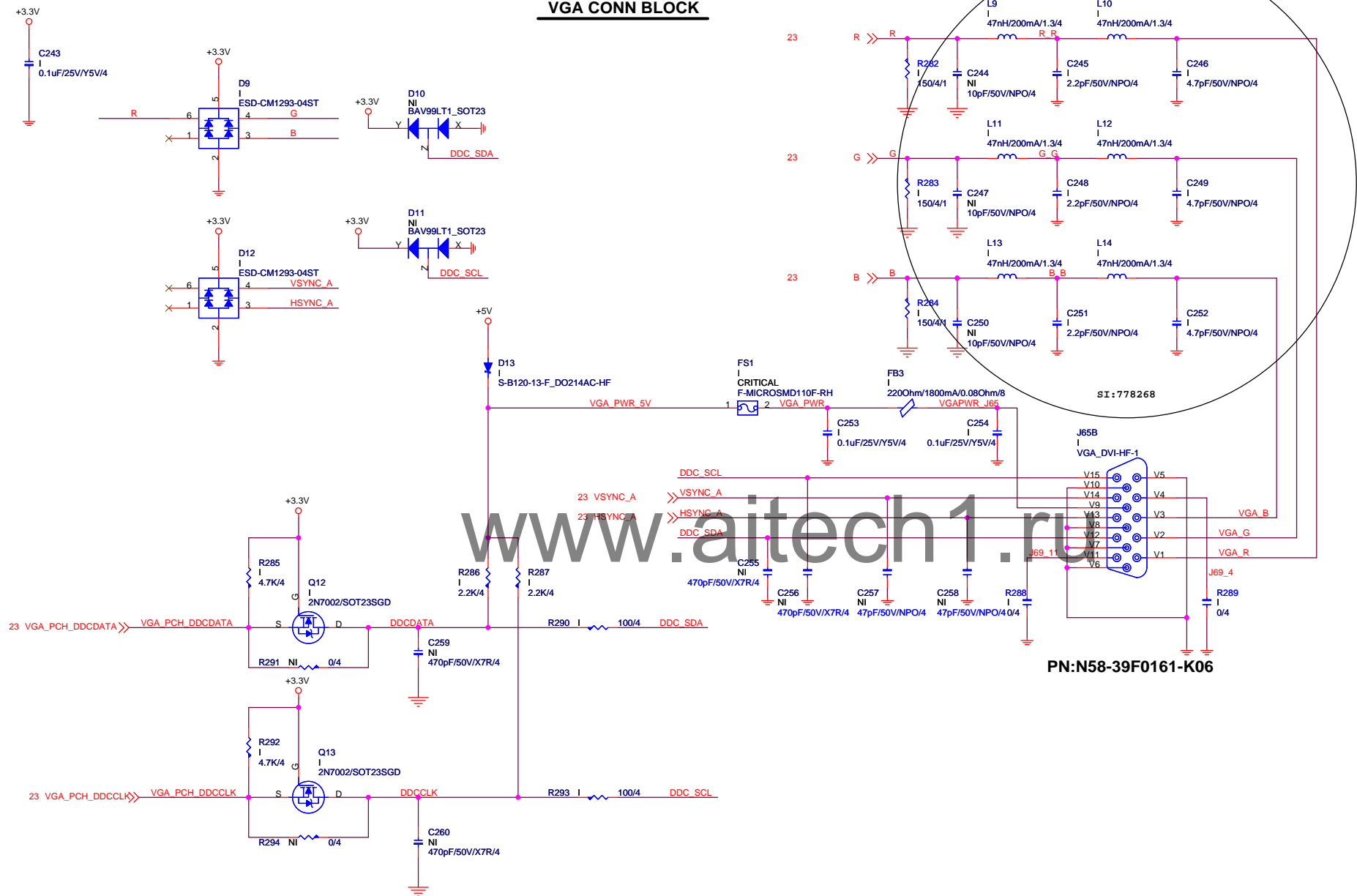
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	PCI pull U D/+3V_SLOT/DPWROK	X2
Date:	Sheet 32 of 63	



# VGA CONN BLOCK



PN:N58-39F0161-K06

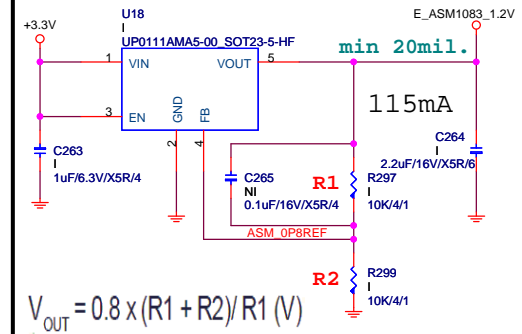
Release Date : Wednesday, November 23, 2011

		<b>MICRO-STAR INT'L CO.,LTD</b>	
<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>		<b>VGA CONN</b>	
Size Custom	Document Description	Rev X2	
Date:		Sheet	33 of 63

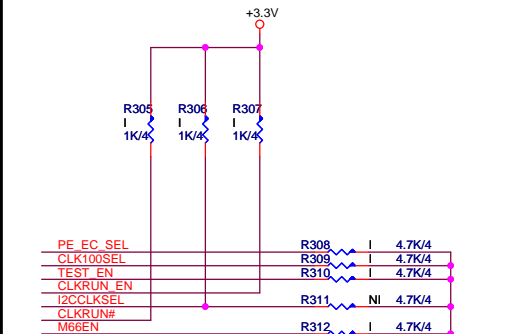
# ASMEDIA/ASM1083

P/N: B0D-0108304-AD0

## E\_ASM1083\_1.2V



## H/W Strapping



PE\_EC\_SEL-  
"H" for Express Card mode  
"L" for PCIe Riser Card mode

CLK100SEL-  
"H" for PECLK input only  
"L" for PECLK & PCICLK input

TEST\_EN-  
"H" for Test Mode Enable  
"L" for Test Mode Disable

CLKRUN\_EN-  
"H" for CLKRUN Mode Disable  
"L" for CLKRUN Mode Enable

I2CCLKSEL-  
"H" is 135KHz I2CCLK  
"L" is 67.5KHz I2CCLK

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ASM1083

ASM1083-RH

3.3V

E\_ASM1083\_1.2V

EMI

Release Date : Wednesday, November 23, 2011

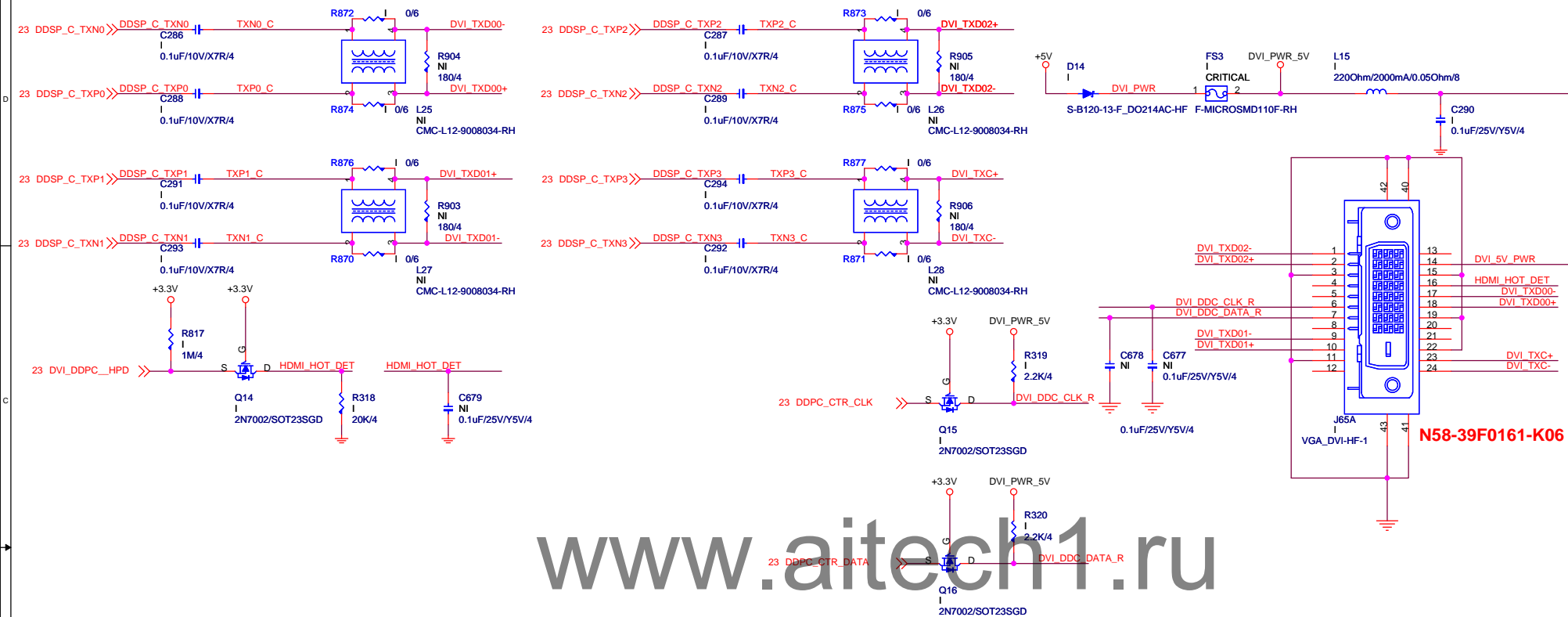


MICRO-STAR INT'L CO.,LTD

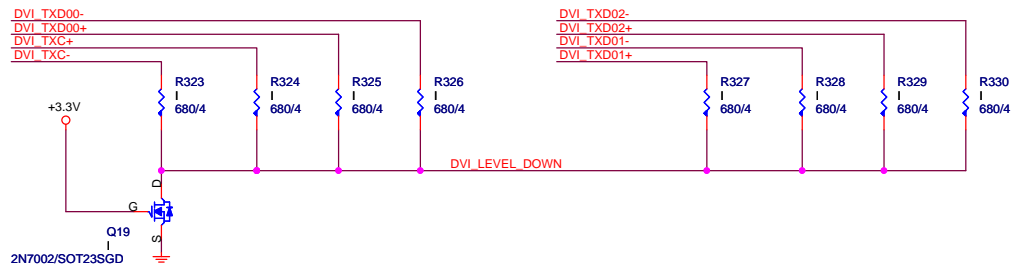
HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	PCIe to PCI Bridge	X2
Date:	Sheet 34 of 63	

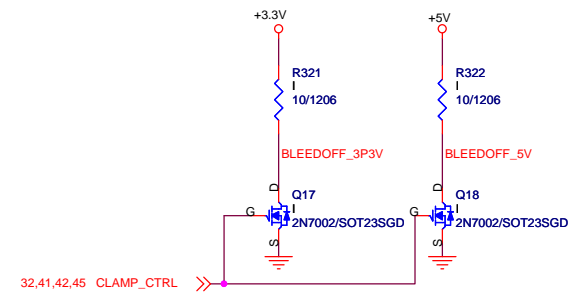
## DVI Connector



## DVI Level Shift



## BLEED-OFF CIRCUIT



**Release Date : Wednesday, November 23, 2011**



**MICRO-STAR INT'L CO.,LTD**

**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size	Document Description
------	----------------------

**DVI / BLEED OFF**

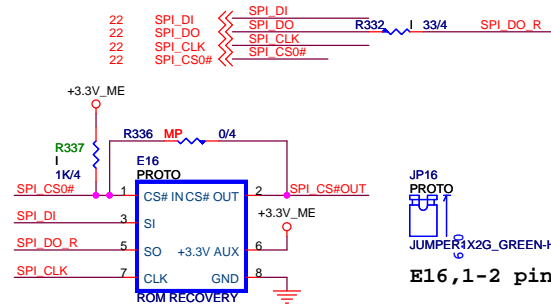
Rev	X2
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Date:	Sheet 35 of 63
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## BIOS

U19  
CRITICAL  
SPI/64Mbit/SOP8

PN:M31-25L6442-M24

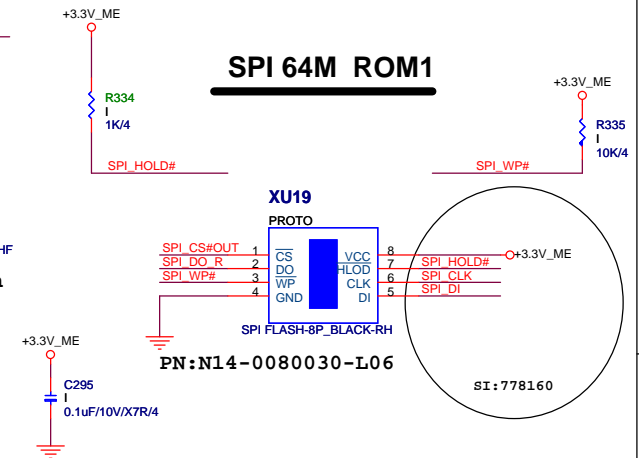


PN:N31-2041261-H06

TABLE 22  
ROM RECOVERY HEADER DEFINITION

E16			
PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	CS# IN	CS# OUT	2
3	SI	KEY (no pin)	4
5	SO	VCC (+3.3V AUX)	6
7	CLK	GND	8

## SPI 64M ROM1



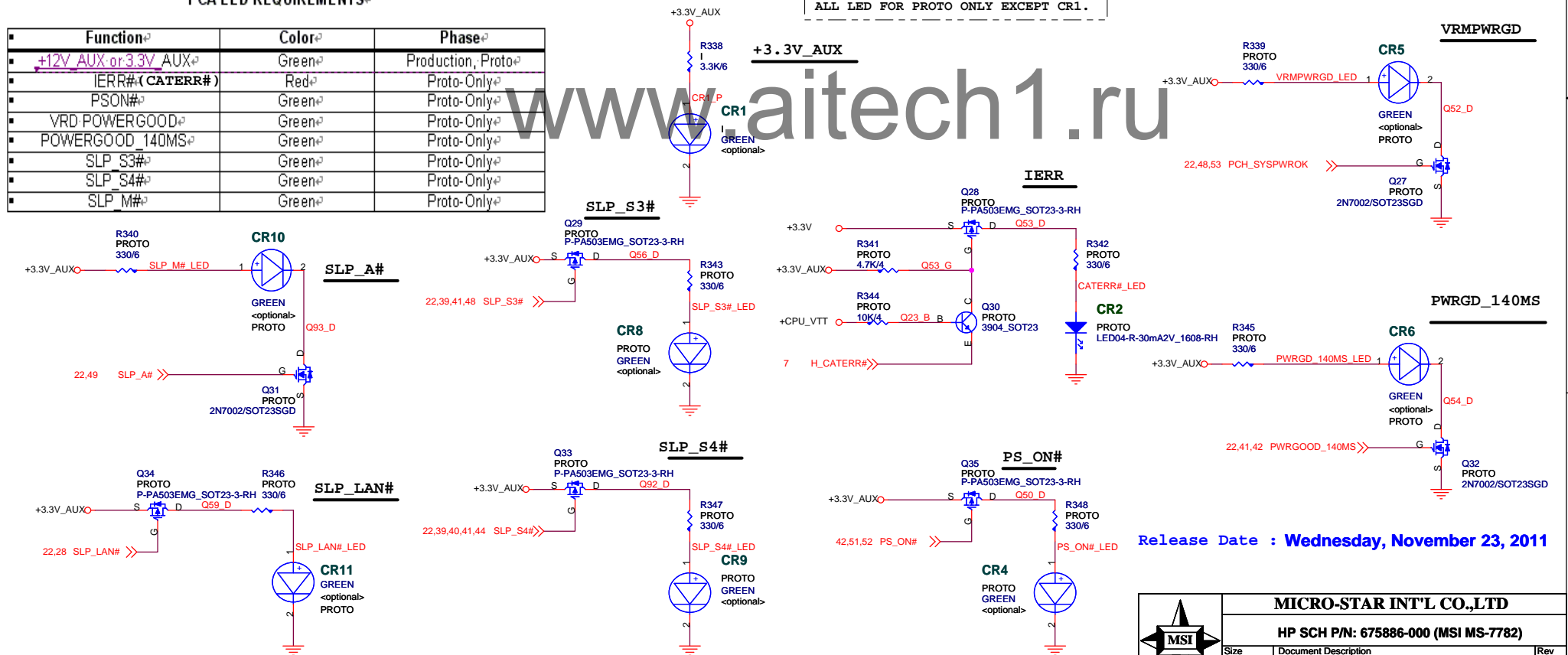
PN:N14-0080030-L06

SI:778160

## PCA LED REQUIREMENTS

Function	Color	Phase
+12V_AUX or 3.3V_AUX	Green	Production, Proto
IERR# (CATERR#)	Red	Proto-Only
PS_ON#	Green	Proto-Only
VRD_POWERGOOD	Green	Proto-Only
POWERGOOD_140MS	Green	Proto-Only
SLP_S3#	Green	Proto-Only
SLP_S4#	Green	Proto-Only
SLP_M#	Green	Proto-Only

[ ALL LED FOR PROTO ONLY EXCEPT CR1. ]



Release Date : Wednesday, November 23, 2011

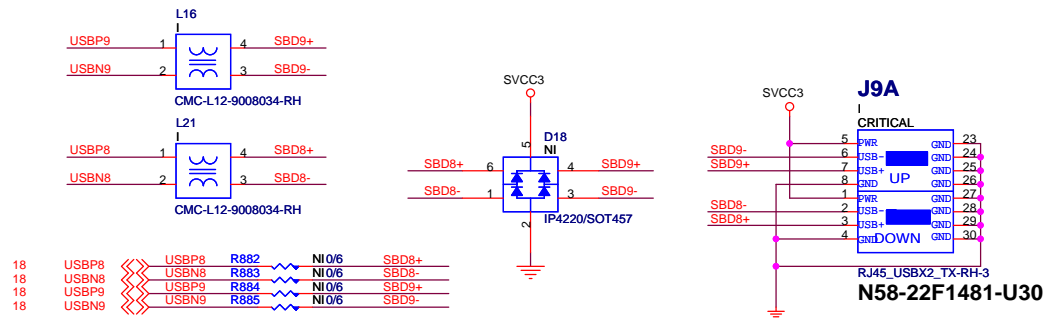


MICRO-STAR INT'L CO.,LTD

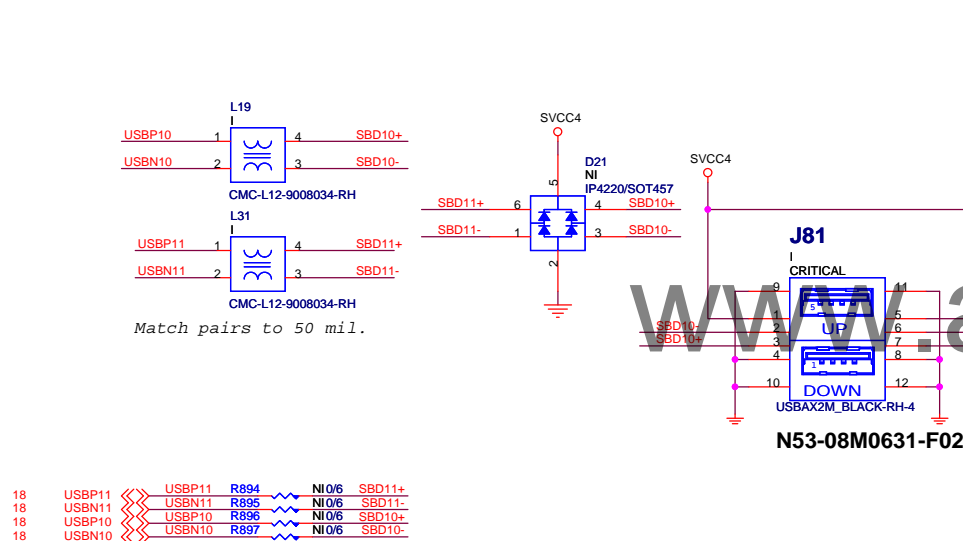
HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	SPI ROM / LED	X2
Date:	Sheet 36 of 63	

## REAL USB CONNECTOR WITH RJ45 FOR USB PORT 8,9



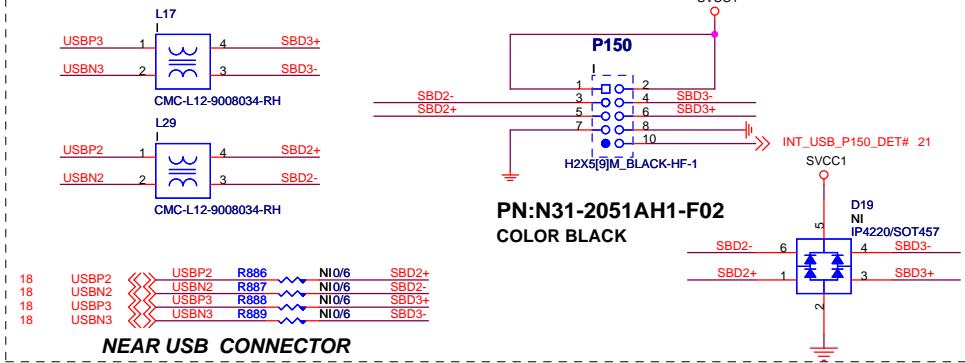
## REAR PANEL USB CONNECTOR FOR USB PORT 10,11



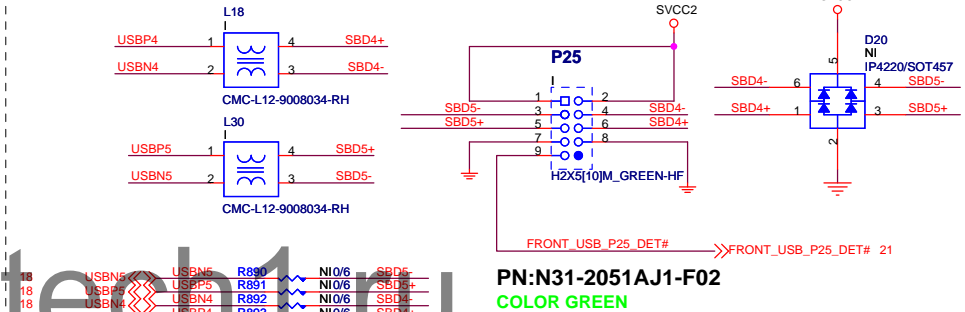
## NEAR USB CONNECTOR



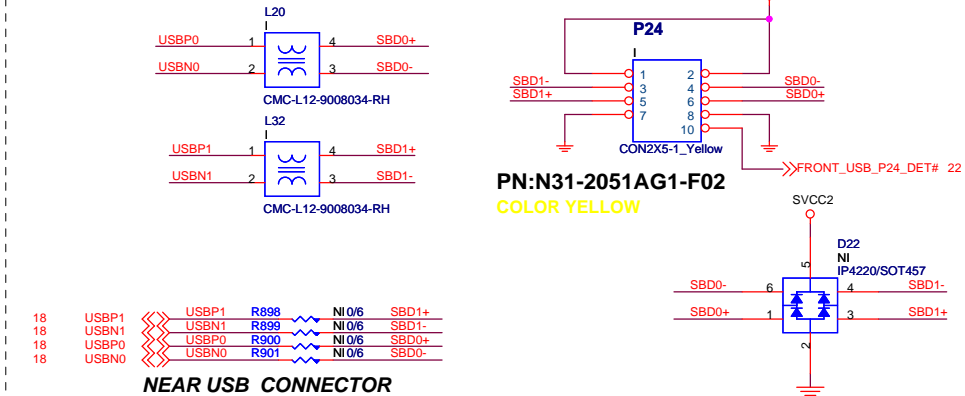
## INTERNAL USB CONNECTOR FOR USB PORT 2,3



## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



## FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



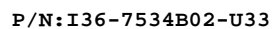
Release Date : Wednesday, November 23, 2011

MICRO-STAR INT'L CO.,LTD	
HP SCH P/N: 675886-000 (MSI MS-7782)	
Size Custom	Document Description
USB Conn.	
Date:	Sheet 37 of 63

P/N: I36-7534B02-U33



P/N: I36-7534B02-U33



P/N: I36-7534B02-U33



**MICRO-STAR INT'L CO.,LTD**

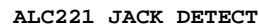
**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size	Document Description
Custom	<a href="#">Eager to Connect</a>

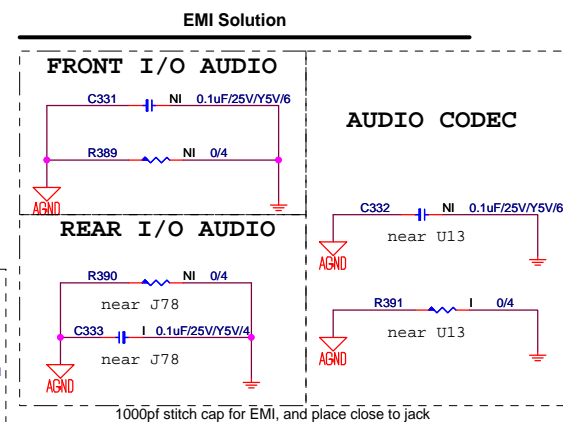
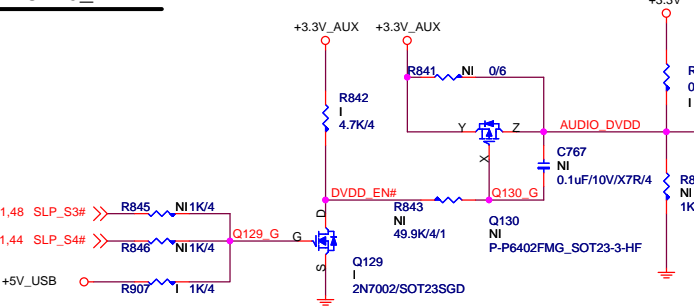
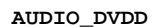
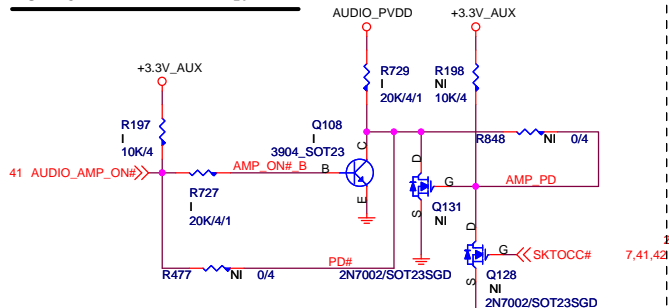
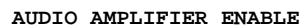
Rev  
yo

Date:	Sheet 38 of 63
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**PN:B05-LC2210C-R09**



All of JD resistors should be placed as close as possible to the sense pin of codec.



**Release Date : Wednesday, November 23, 2011**



**MICRO-STAR INT'L CO.,LTD**

**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size	Document Description
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Size	Document Description
Custom	<b>ALC 221 CODEC</b>

	Re
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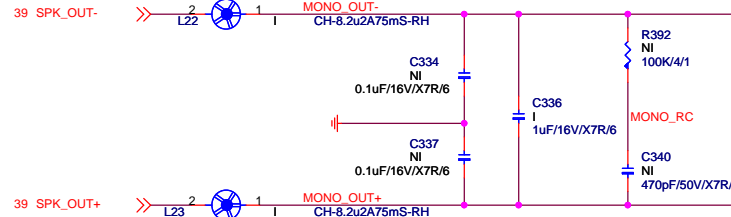
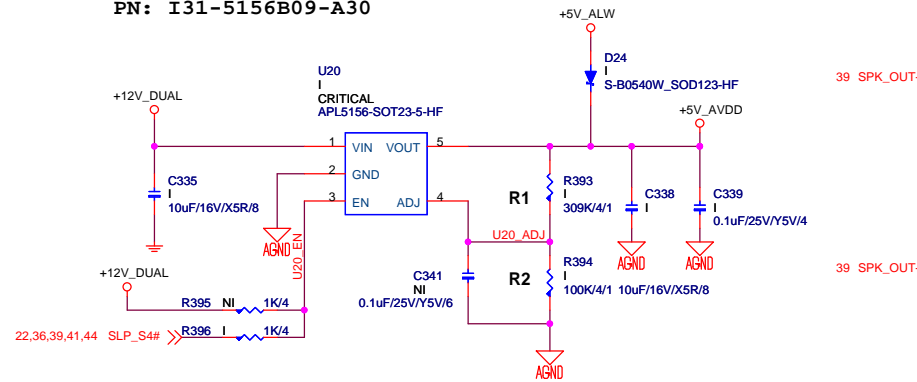
Date:	Sheet 39 of 63
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# AUDIO CODEC REGULATORS

PN: I31-5156B09-A30

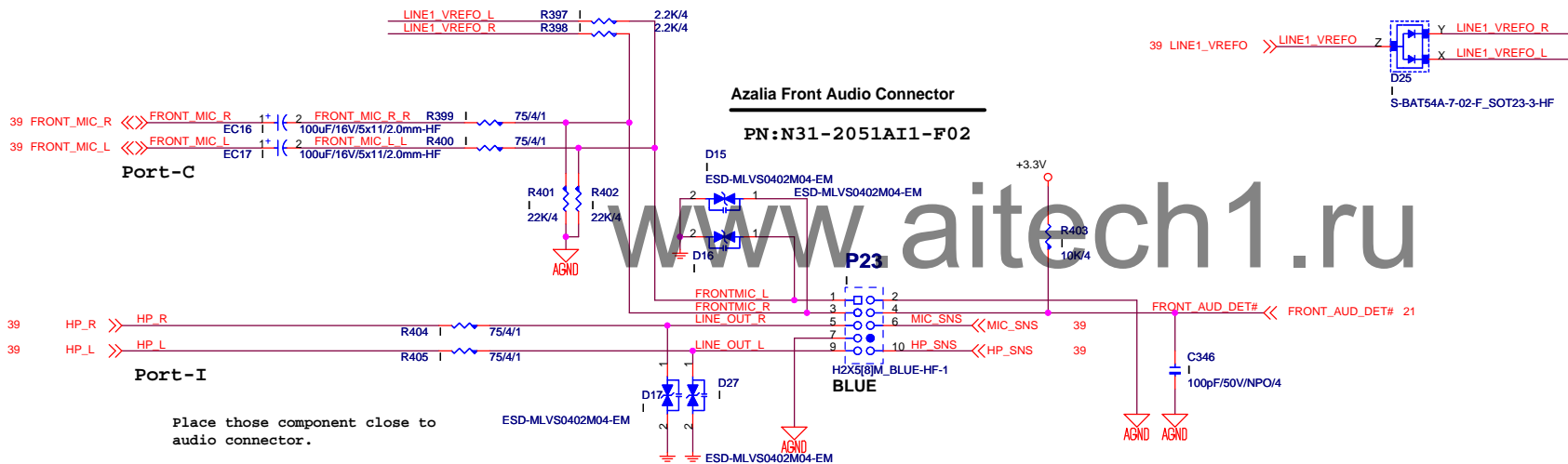
# SPEAKER HEADER

P/N:N32-10200D1-F02

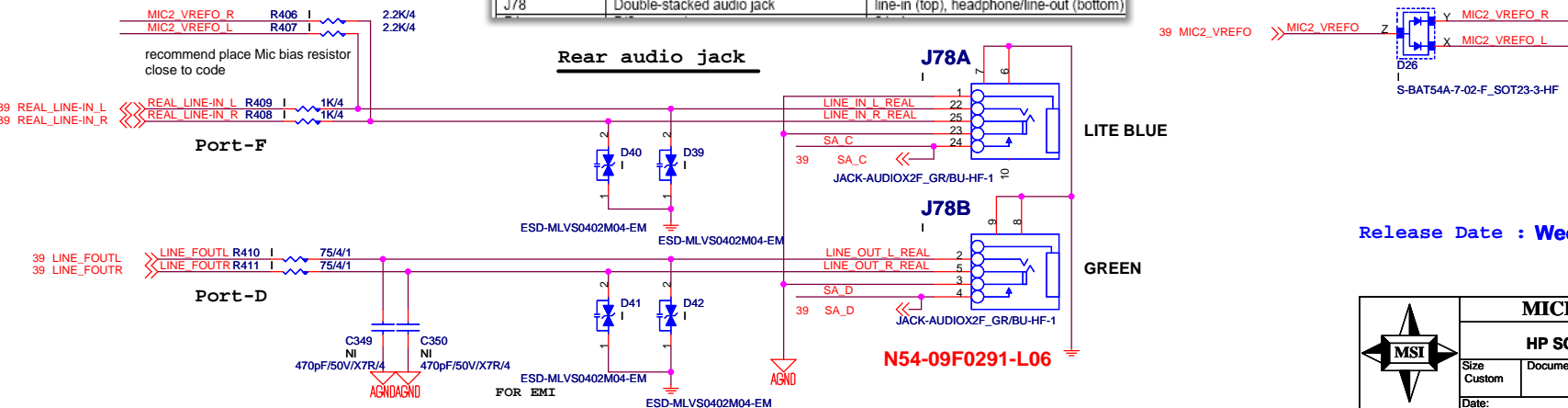


SPK+- TRACE WIDTH  
Speaker 4 ohm ==> 40mils  
Speaker 8 ohm ==> 20mils

TABLE 14 SPEAKER HEADER DEFINITION	
P6	
SPEAKER-	1
SPEAKER+	2



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Release Date : Wednesday, November 23, 2011

MICRO-STAR INT'L CO.,LTD	
HP SCH P/N: 675886-000 (MSI MS-7782)	
Size Custom	Document Description
Audio Connector	
Date:	Rev X2
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PN:B02-0379H04-NX9



Size Custom	Document Description <b>LPC SUPER I/O NPCD379H</b>	Rev X2
Date:	Sheet 41 of 63	

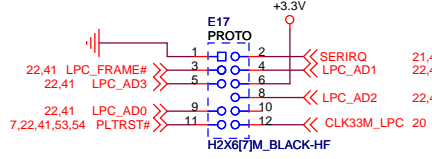
SYSOPT Strap (RTS1-):  
R124 - 0x2E\* DEFAULT  
R144 - 0x4E

- No pull-down resistor (default) - normal device operation.  
- 4.7 K $\Omega$  external pull-down resistor- JTAG selected.

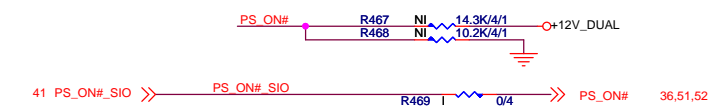
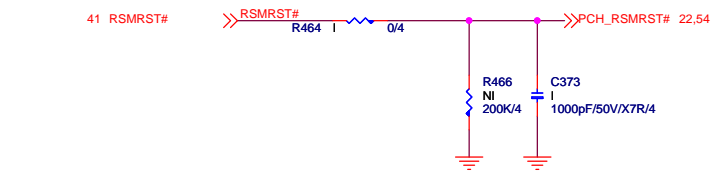
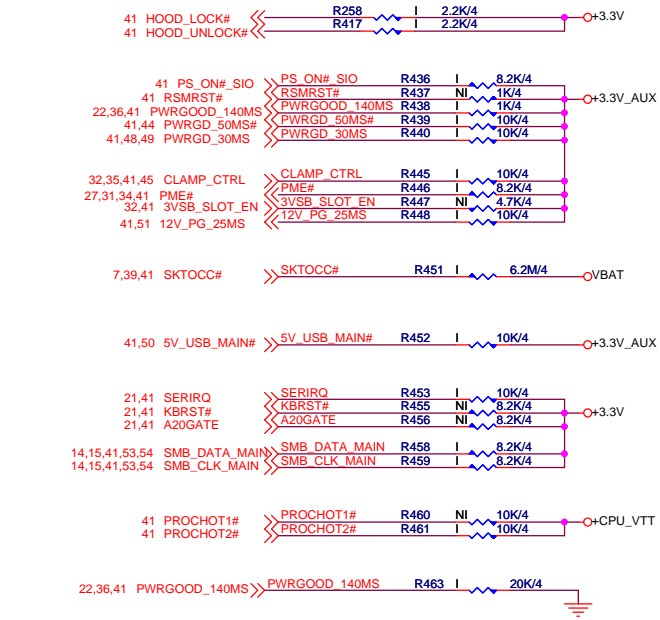
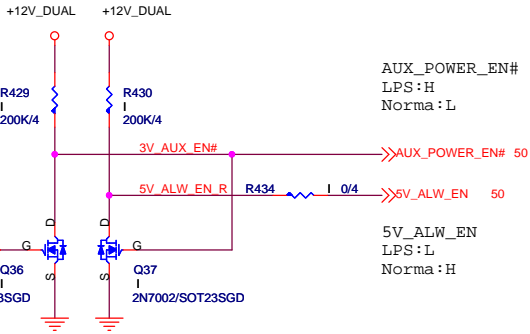
- 10 K $\Omega$  external pull-up resistor - Workstations pins default.  
- 10 K $\Omega$  external pull-down resistor - Desktop pins default.

- No pull-down resistor (default) - normal pin operation.  
- 4.7 K $\Omega$  external pull-down resistor - floating device pins.

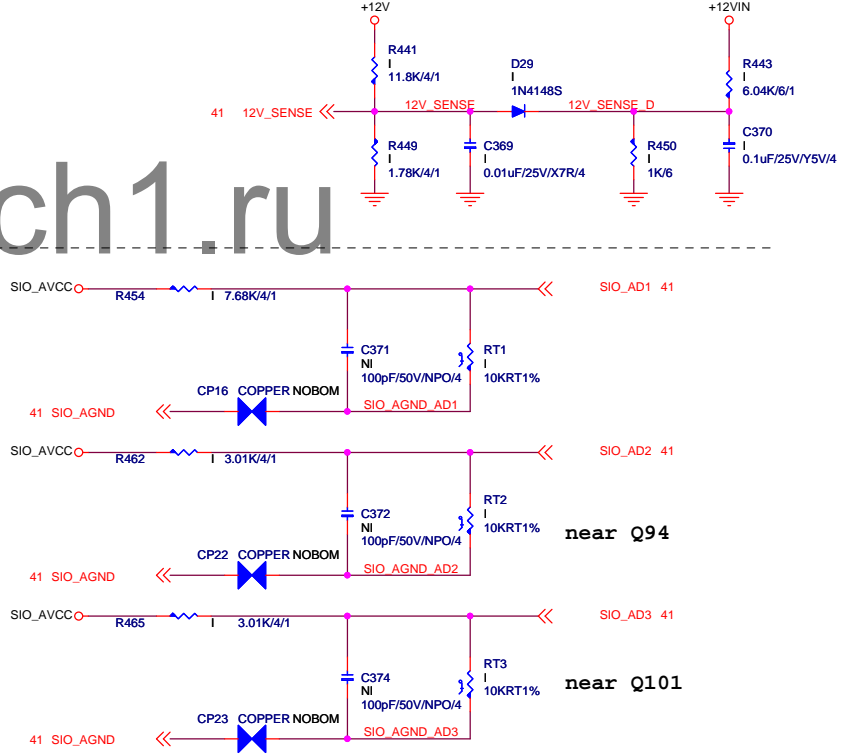
LPC Debug



SI:780764 N31-2061311-H06



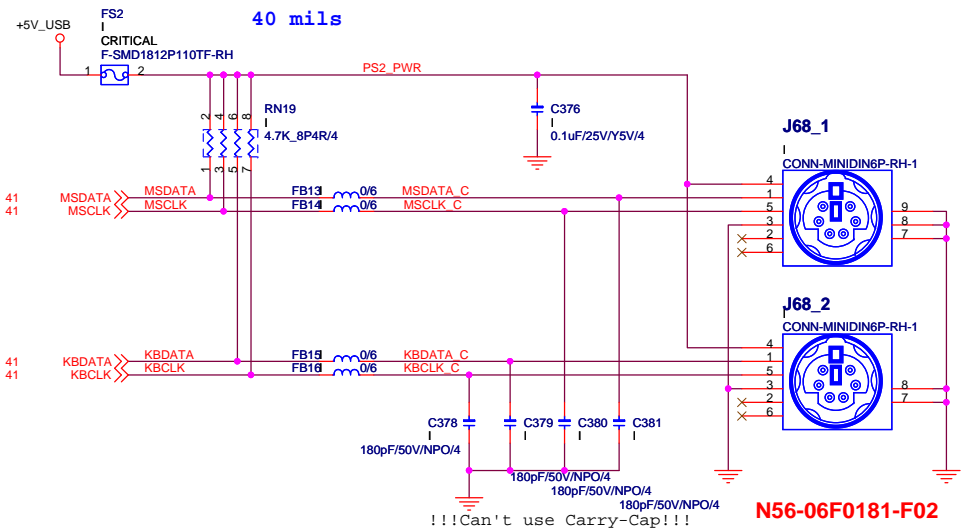
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Release Date : Wednesday, November 23, 2011

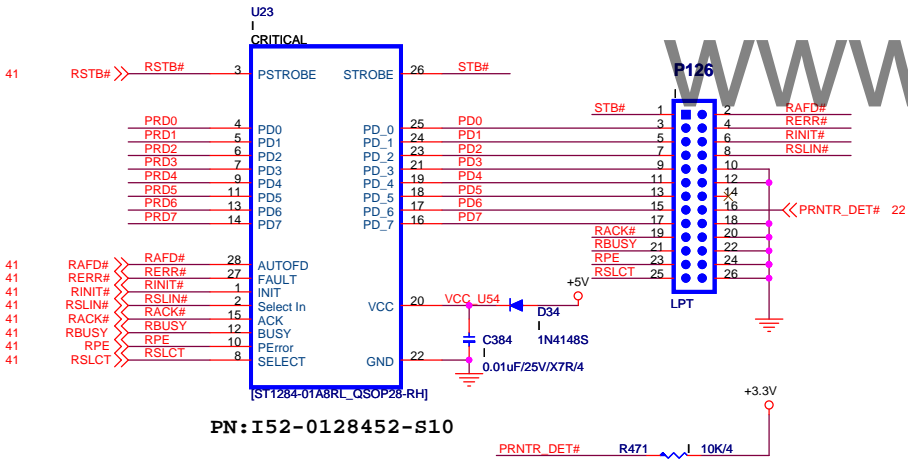
	<b>MICRO-STAR INT'L CO.,LTD</b>			
	<b>HP SCH P/N: 675886-000 (MSI MS-7782)</b>			
	Size Custom	Document Description		Rev X2
		<b>SIO PULL UP/DOWN</b>		
	Date:		Sheet 42 of	63

PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT

PN:N31-2131191-F02

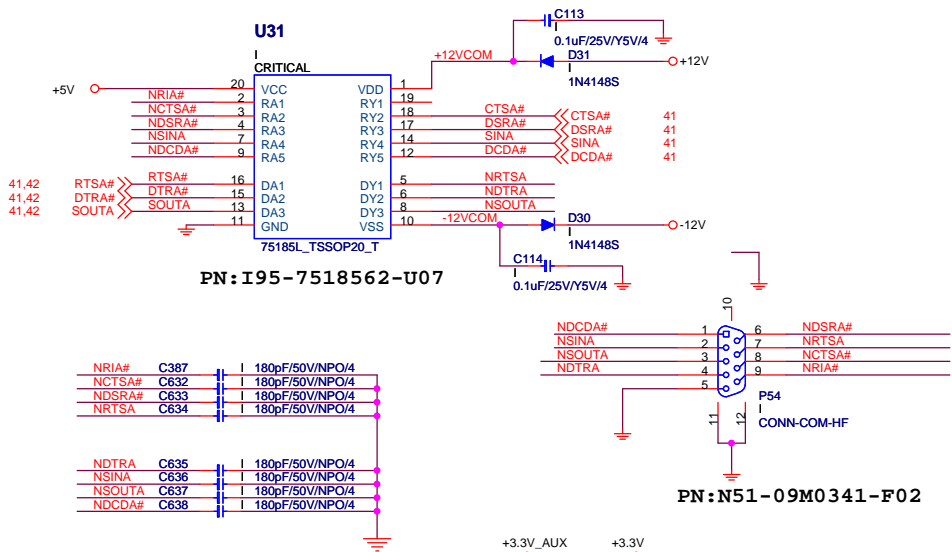


PN:I52-0128452-S10

Parallel Port 2 x13 header

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	LPT_STB#	XAFD#	2
3	LPT_SPD0	ERROR#	4
5	LPT_SPD1	XINIT#	6
7	LPT_SPD2	XSLIN#	8
9	LPT_SPD3	GND	10
11	LPT_SPD4	GND	12
13	LPT_SPD5	GND	14
15	LPT_SPD6	PRT_DET#	16
17	LPT_SPD7	GND	18
19	ACK#	GND	20
21	BUSY	GND	22
23	SLCT	LDT_RST#	24
		GND	26

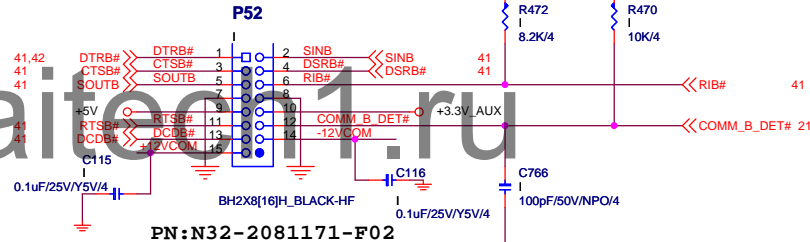
SERIAL PORT 1



PN:I95-7518562-U07

PN:N51-09M0341-F02

SERIAL PORT 2



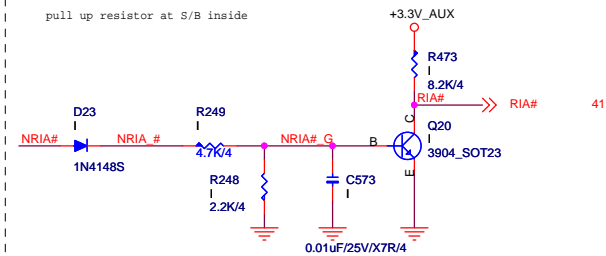
PN:N32-2081171-F02

TABLE 12  
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	R#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

Support ring wake up

pull up resistor at S/B inside



Release Date : Wednesday, November 23, 2011

**MICRO-STAR INT'L CO.,LTD**

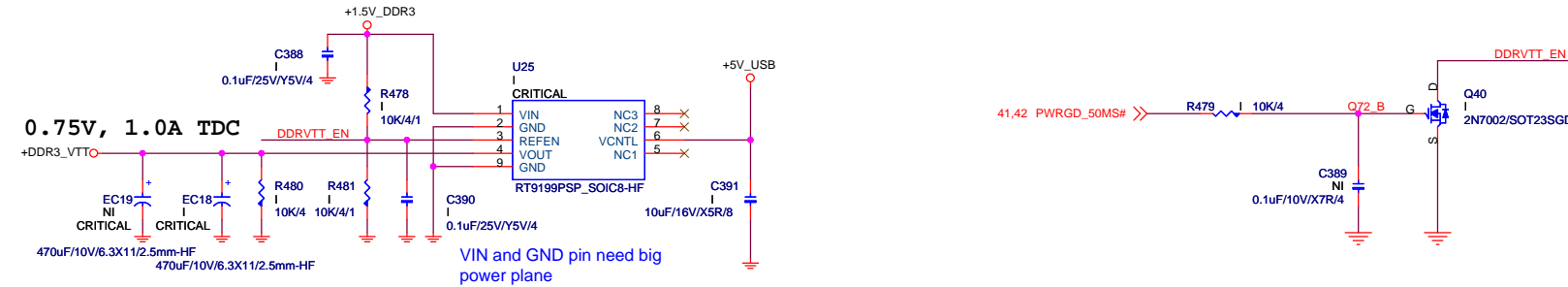
**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size Custom Document Description  
**KB / MS / COM / LPT**

Date: Sheet 43 of 63

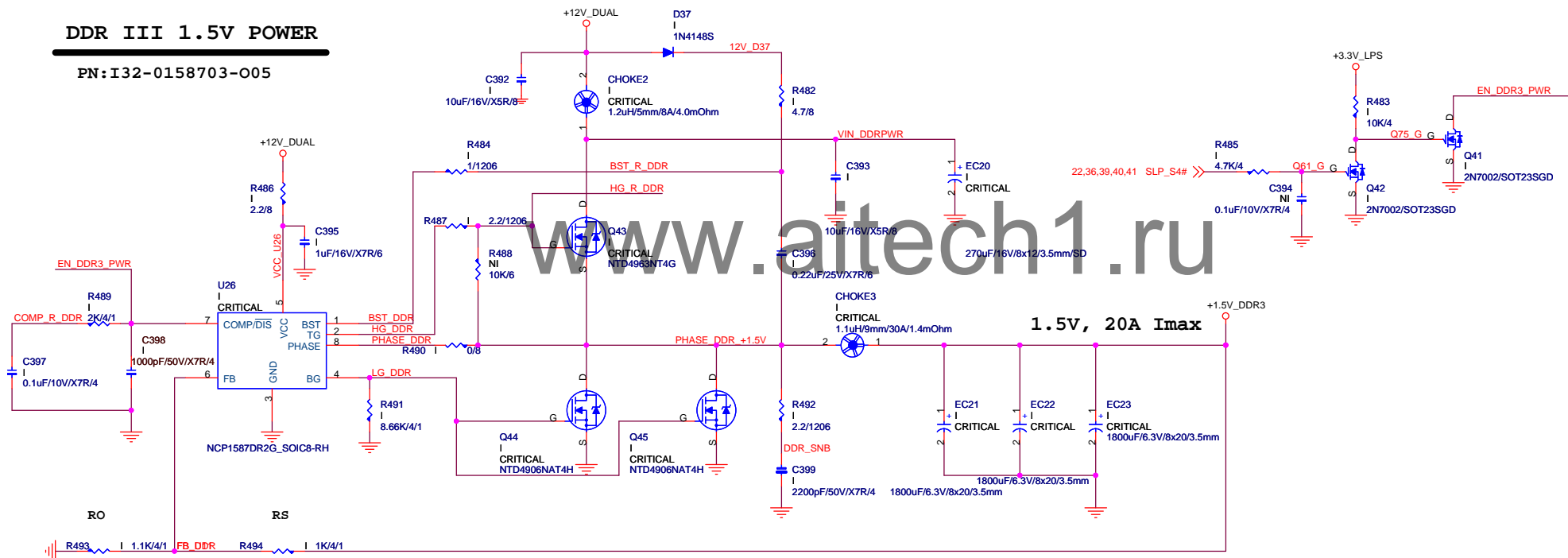
## DDR VTT Power

PN: I31-0919902-R11

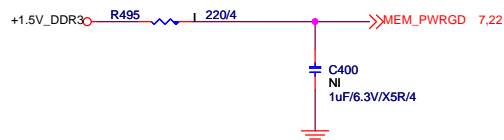


## DDR III 1.5V POWER

PN: I32-0158703-O05



## MEM\_PWRGD



Release Date : Wednesday, November 23, 2011



MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

Size  
Custom

Document Description  
+1.5V\_DDR3 / DDRVTT

Rev  
X2

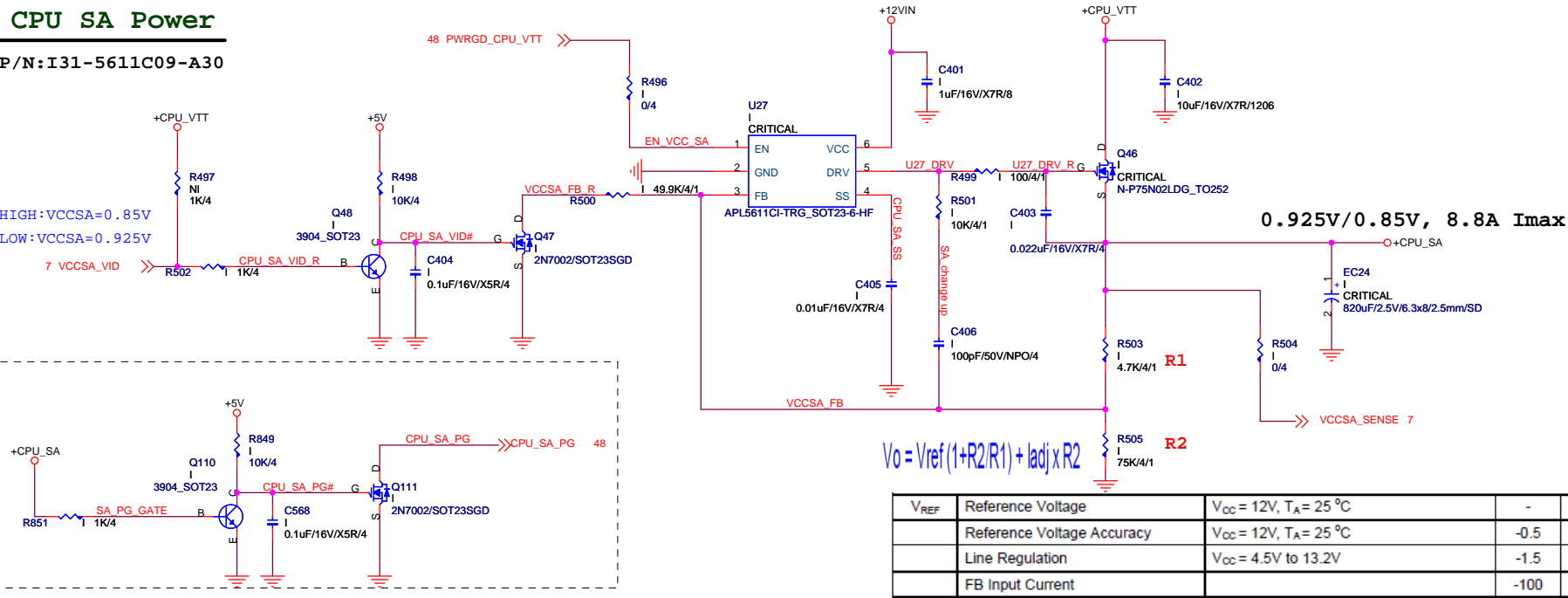
Date:

Sheet 44 of 63

# CPU SA Power

P/N: I31-5611C09-A30

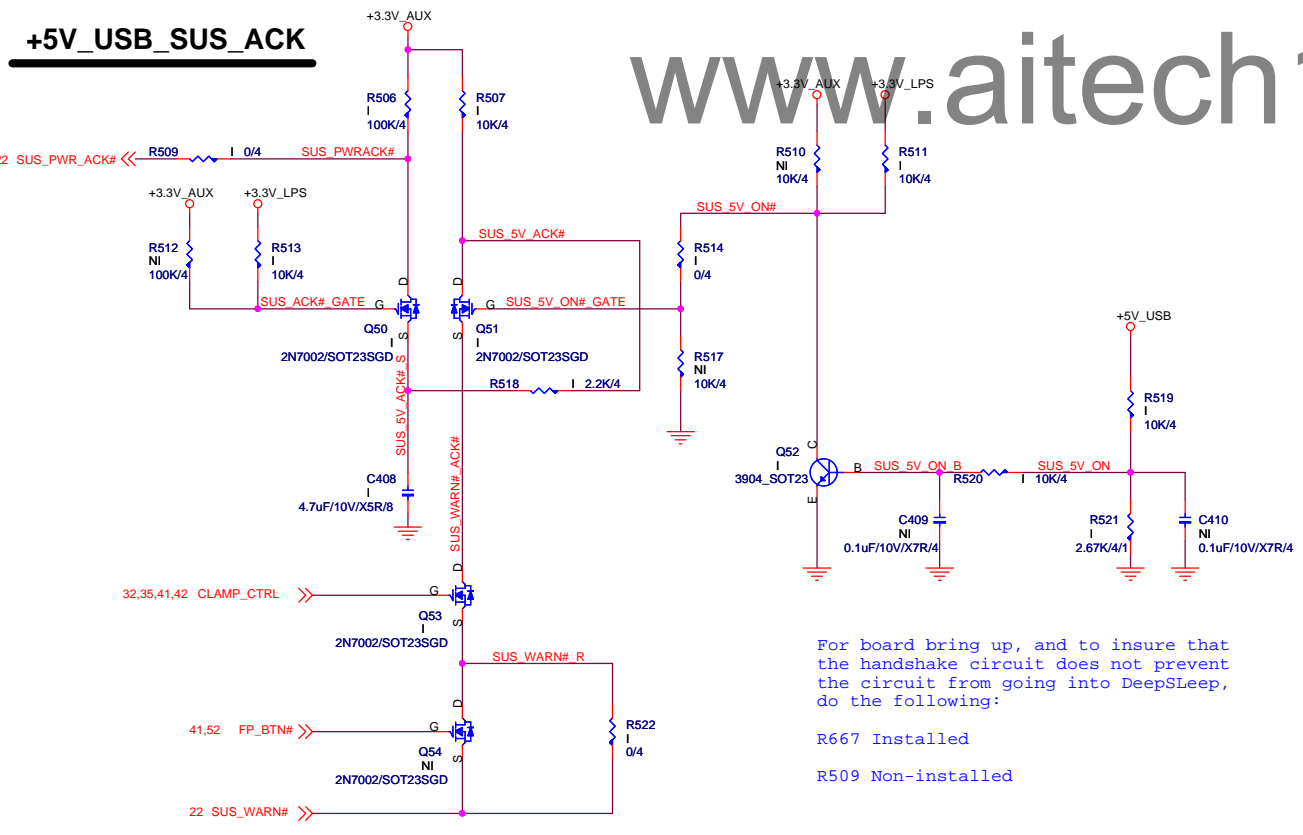
HIGH: VCCSA=0.85V  
LOW: VCCSA=0.925V



$$V_o = V_{ref}(1+R_2/R_1) + I_{adj} \times R_2$$

V <sub>REF</sub>	Reference Voltage	V <sub>CC</sub> = 12V, T <sub>A</sub> = 25 °C	-	0.8	-	V
	Reference Voltage Accuracy	V <sub>CC</sub> = 12V, T <sub>A</sub> = 25 °C	-0.5	-	0.5	%
	Line Regulation	V <sub>CC</sub> = 4.5V to 13.2V	-1.5	-	1.5	%
	FB Input Current		-100	-	100	nA

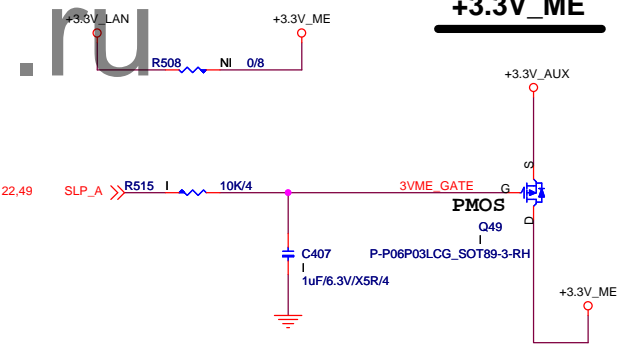
## +5V\_USB\_SUS\_ACK



For board bring up, and to insure that the handshake circuit does not prevent the circuit from going into DeepSleep, do the following:

- R667 Installed
- R509 Non-installed

## +3.3V\_ME



Release Date : Wednesday, November 23, 2011

**MICRO-STAR INT'L CO.,LTD**

**HP SCH P/N: 675886-000 (MSI MS-7782)**

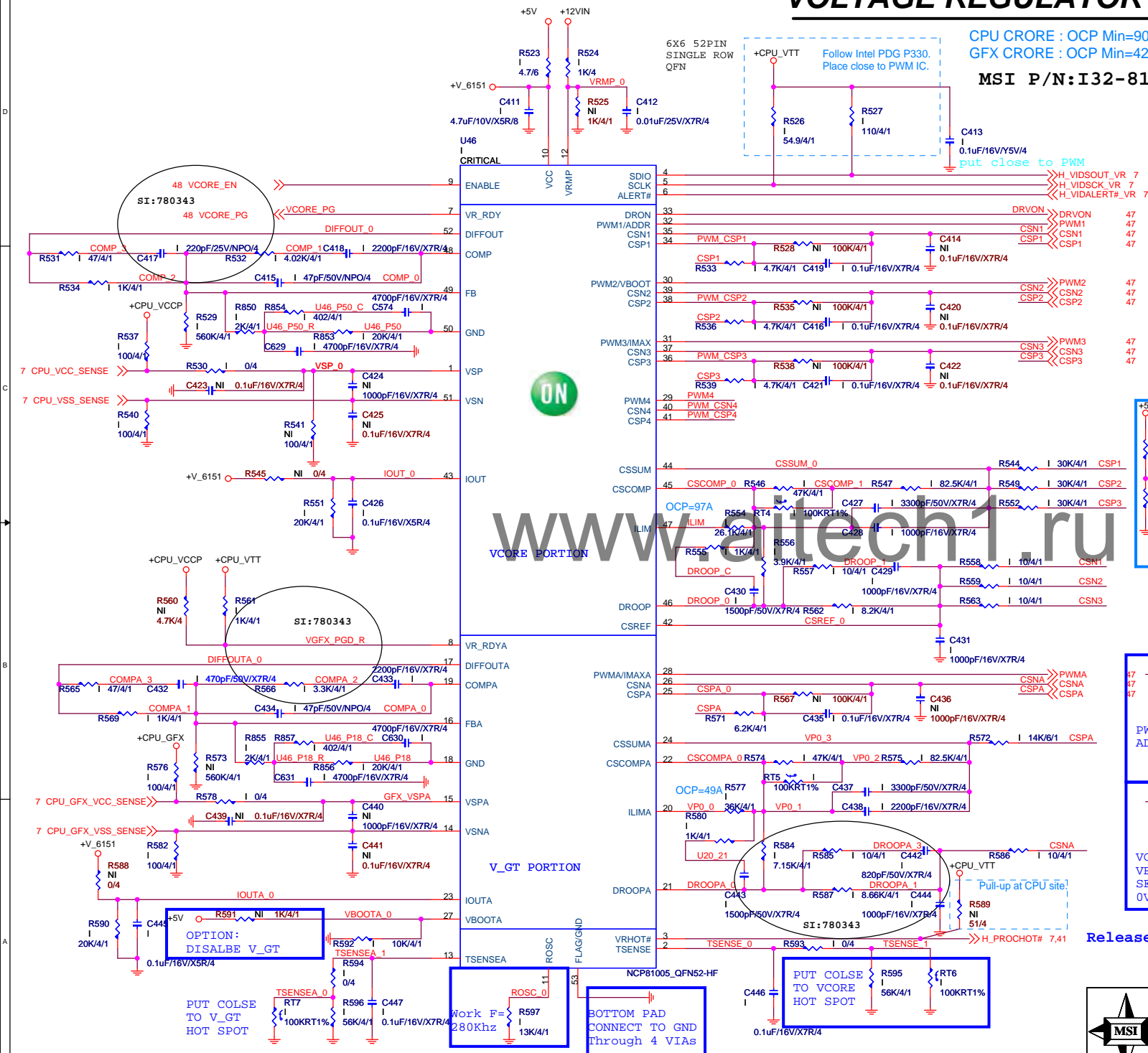
Size Custom Document Description **CPU SA POWER/4.3V\_ME** Rev X2

Date: Sheet 45 of 63

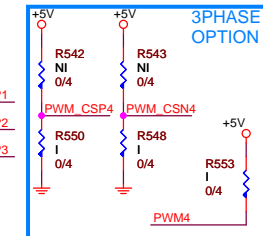
## VOLTAGE REGULATOR MODULE (VRD12)

CPU CRORE : OCP Min=90A , OCP Max=108A , OVP=DAC+175mV  
GFX CRORE : OCP Min=42A , OCP Max=52.5A , OVP=DAC+175mV

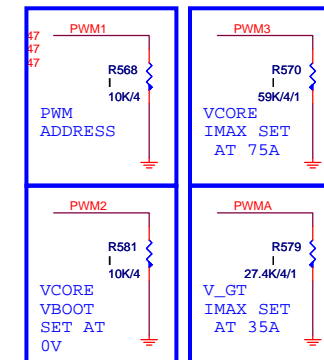
MSI P/N:I32-810050C-005



PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101



BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V



Release Date : Wednesday, November 23, 2011

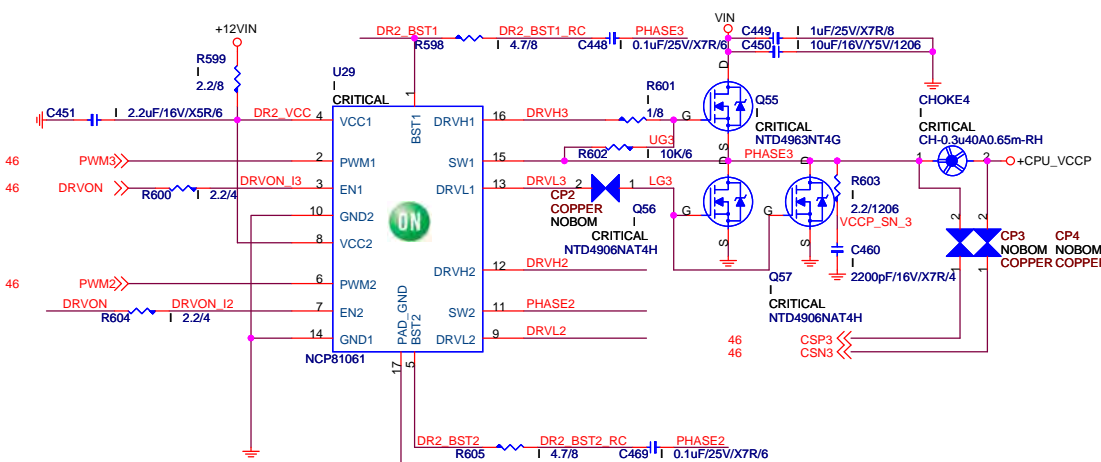


**MICRO-STAR INT'L CO.,LTD**

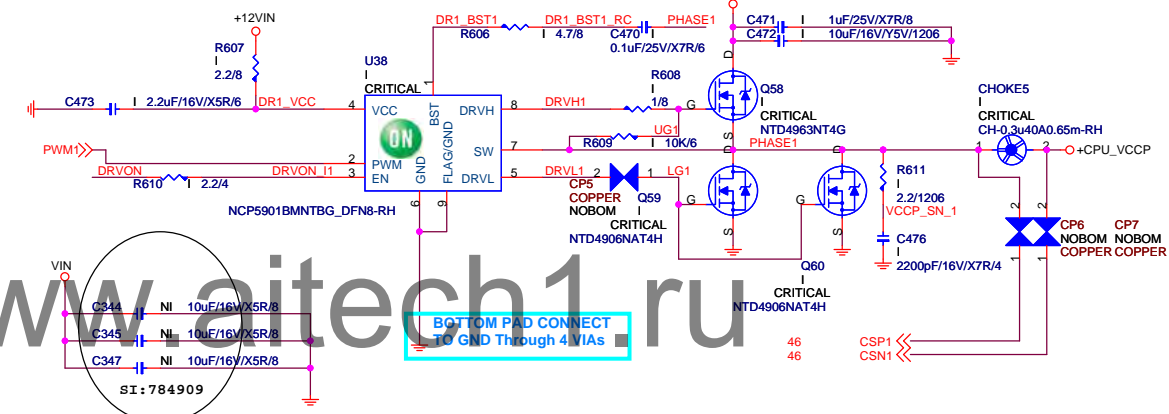
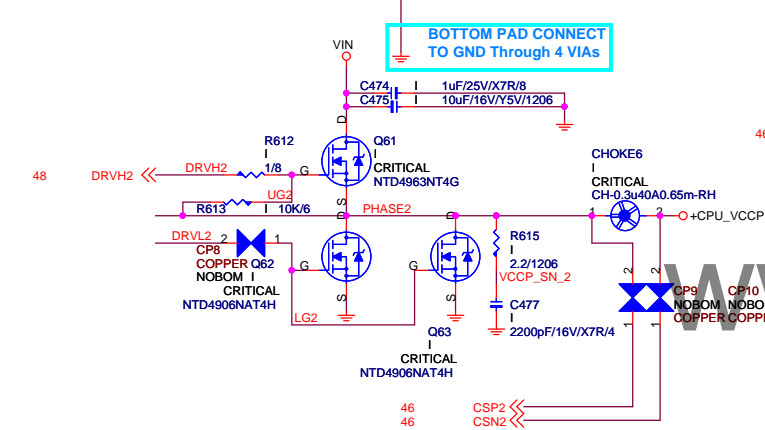
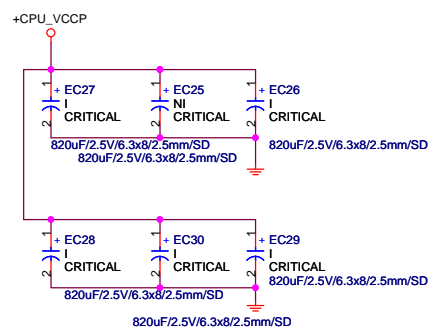
**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size Custom	Document Description <b>VRM-NCP81005</b>	Rev X2
Date:	Sheet 46 of 63	

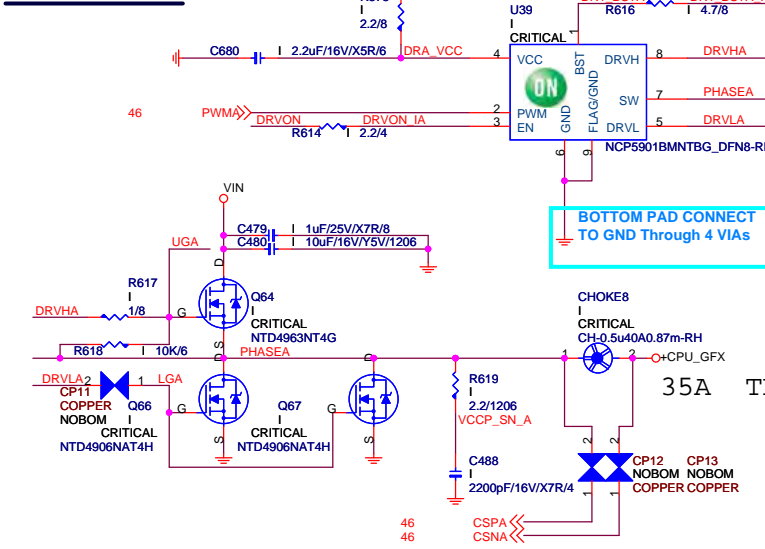




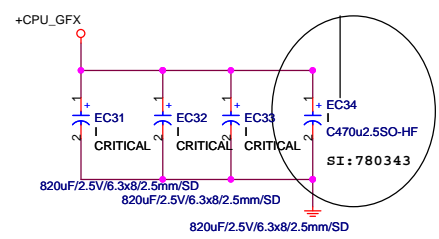
# +CPU\_VCCP Output Caps



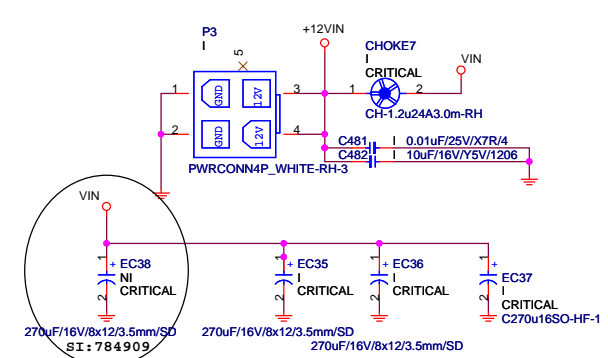
# +CPU\_GFX



# Place bottom side



# ATX12V Power Connector



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HP SCH P/N: 675886-000 (MSI MS-7782)

Document Description  
VRM DRIVER-NCP81061

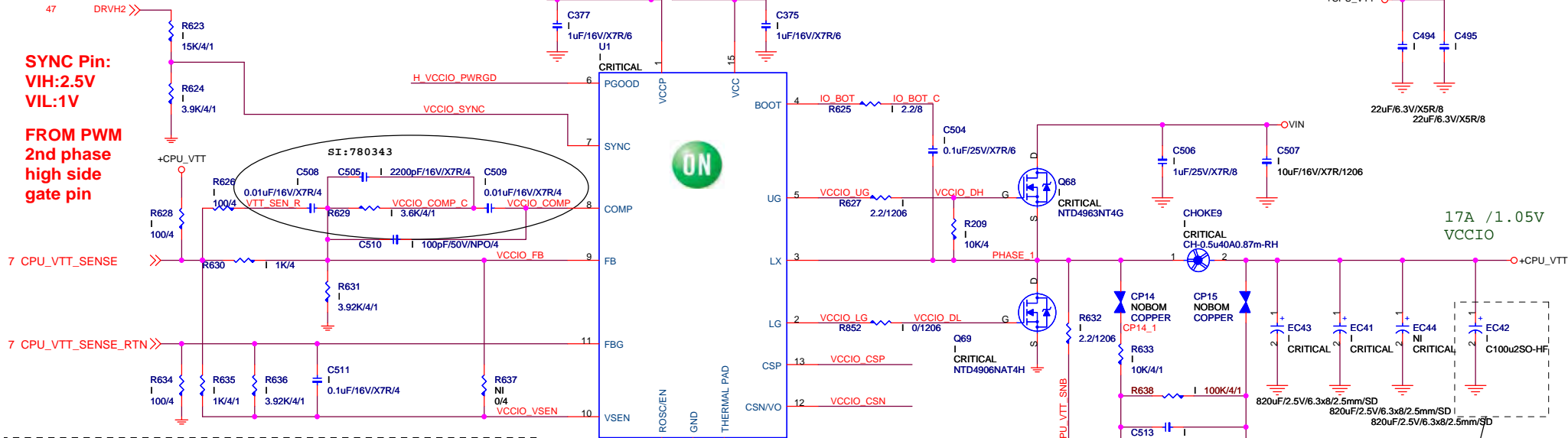
Date: Sheet 47 of 63

## CPU VTT Power

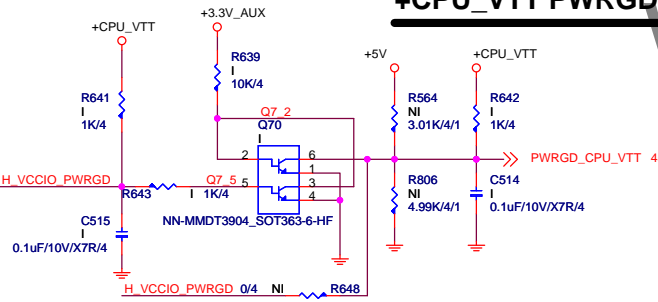
P/N: I32-5230M0C-O05

SYNC Pin:  
VIH:2.5V  
VIL:1V

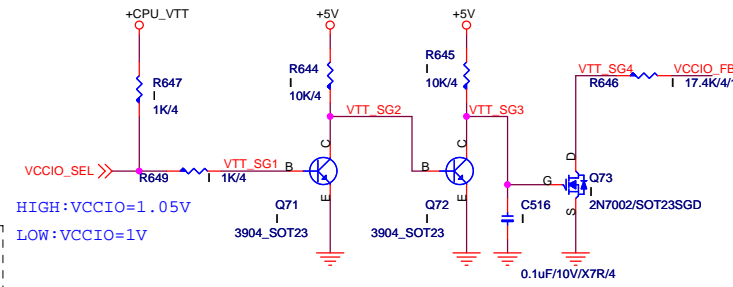
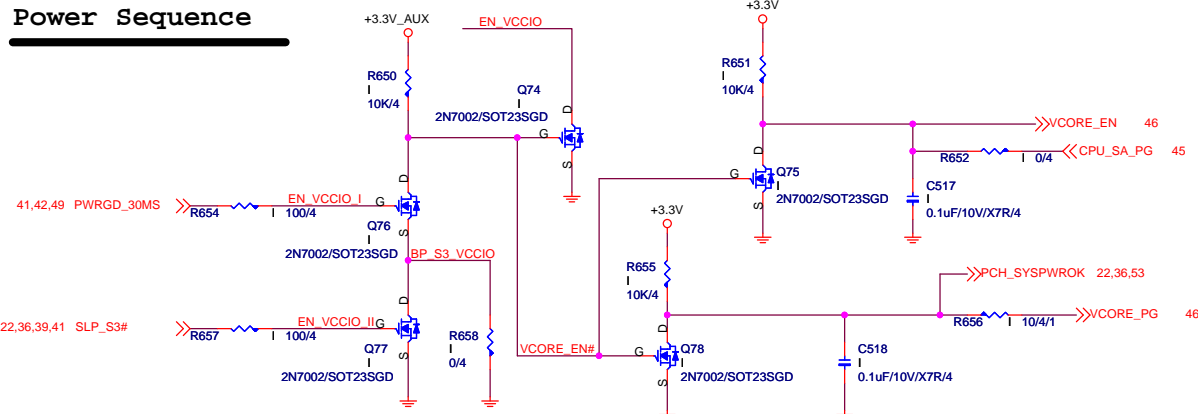
FROM PWM  
2nd phase  
high side  
gate pin



+CPU\_VTT PWRGD



## Power Sequence

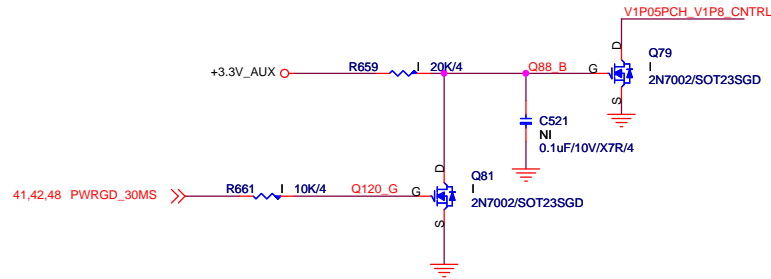


Release Date : Wednesday, November 23, 2011

MICRO-STAR INT'L CO.,LTD			
HP SCH P/N: 675886-000 (MSI MS-7782)			
Size	Document Description	Rev	
Custom	CPU VTT POWER	X2	
Date:		Sheet	48 of 63

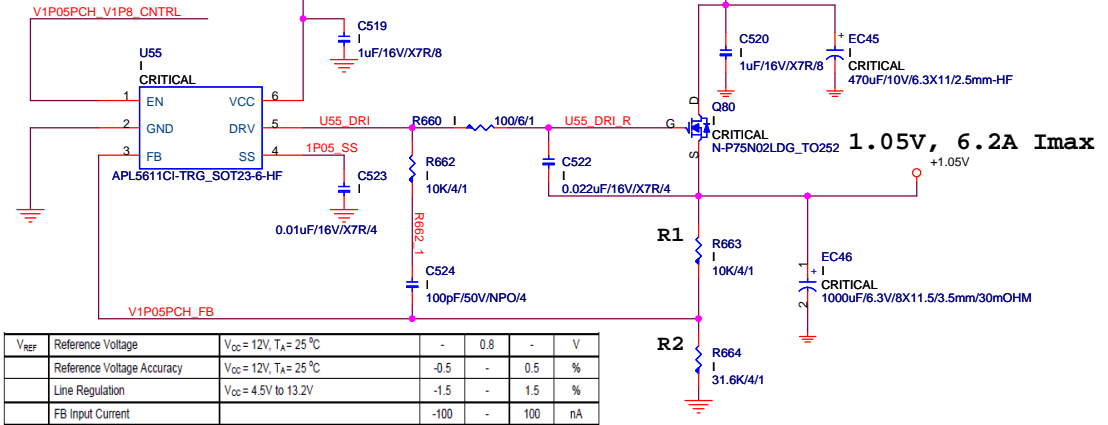


# V1P05PCH\_CNTRL\_INPUT V1P8\_CNTRL\_INPUT

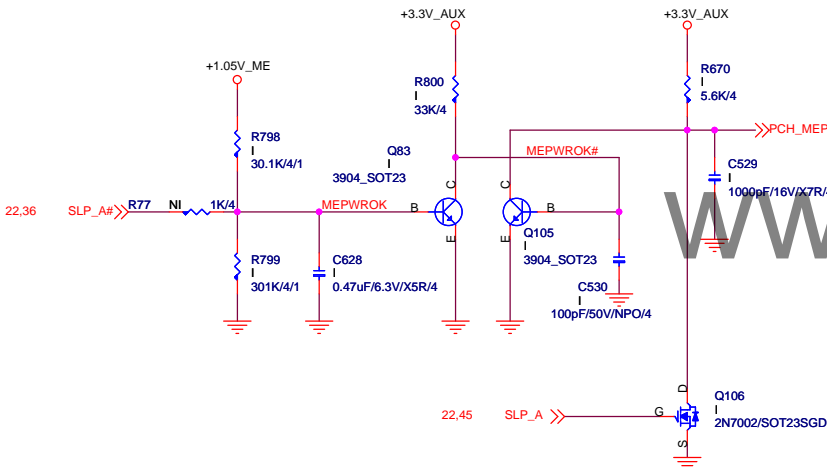


## +1.05V

PN: I31-5611C09-A30

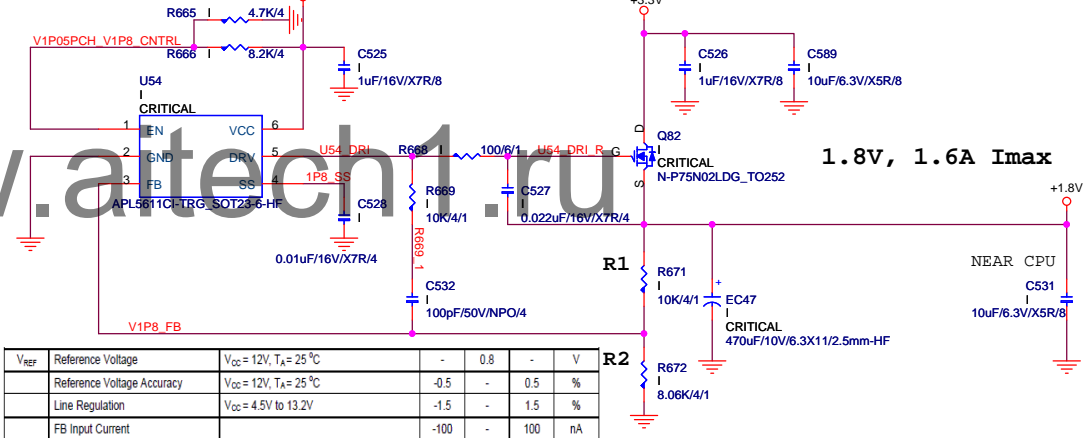


## PCH MEPWROK



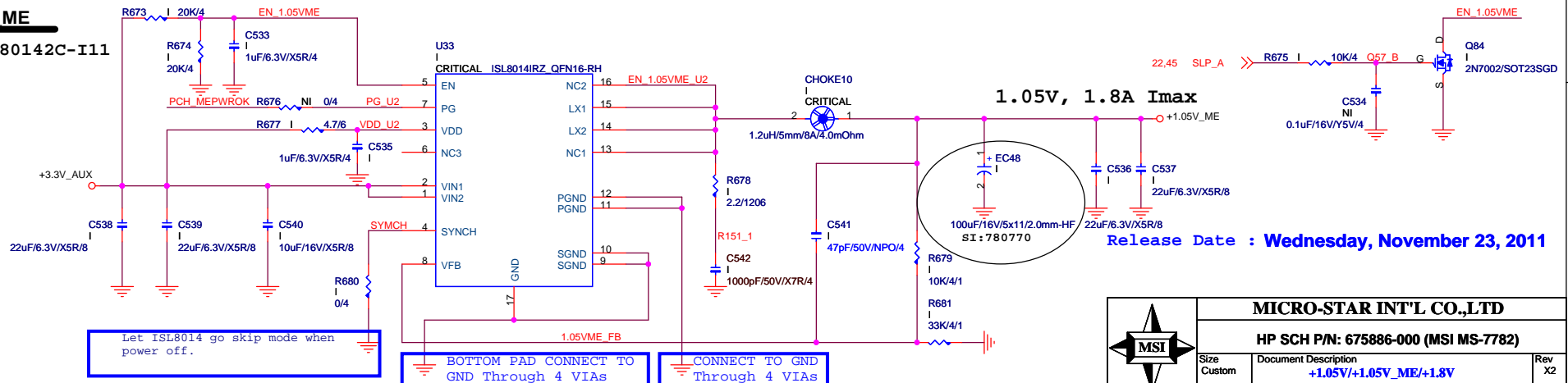
## +1.8V

PN: I31-5611C09-A30



## +1.05V ME

PN: I32-080142C-I11



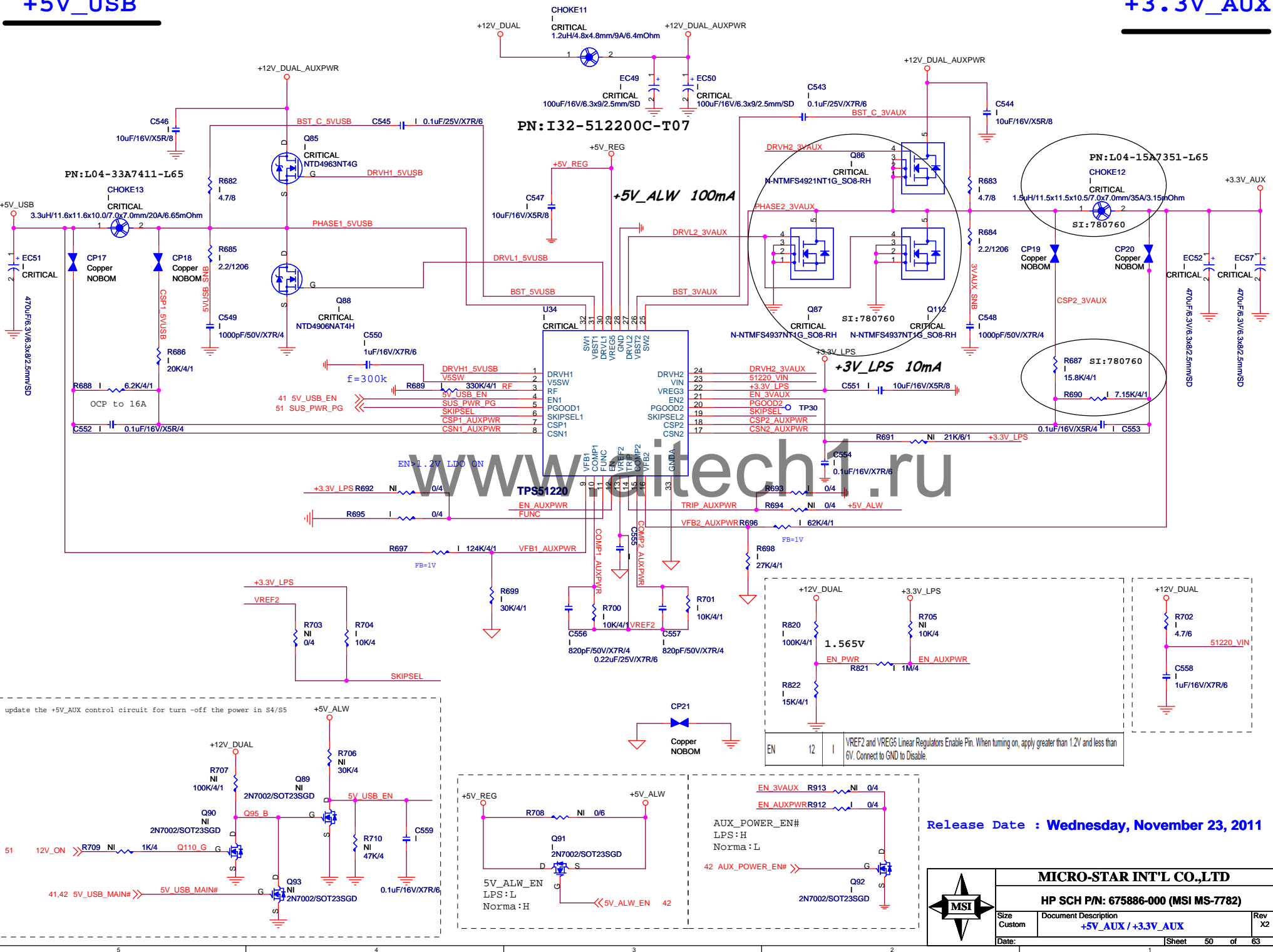
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 675886-000 (MSI MS-7782)

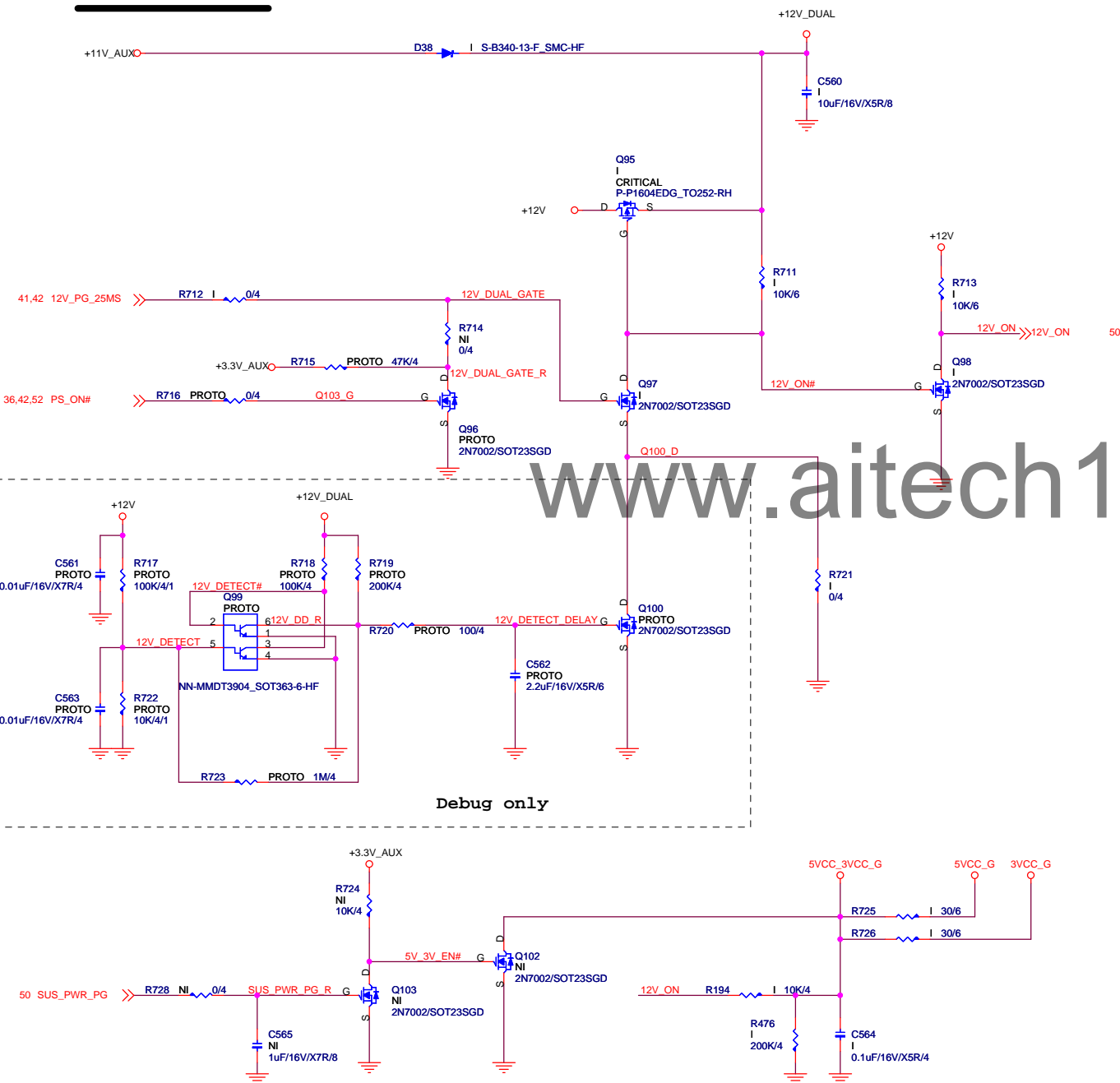
Size Custom	Document Description	Rev X2
	+1.05V/+1.05V_ME/+1.8V	
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+5V\_USB

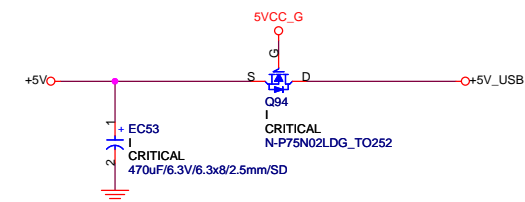
+3.3V\_AUX



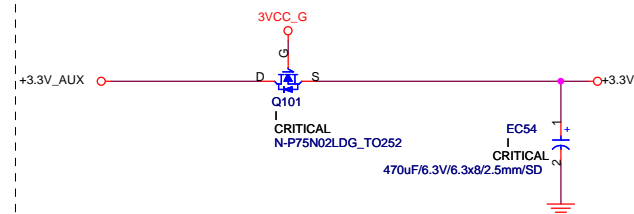
## +12V\_DUAL



## +5V



## +3.3V



Release Date : Wednesday, November 23, 2011

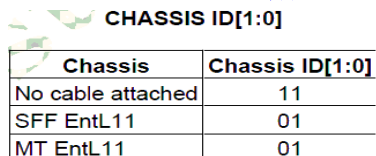


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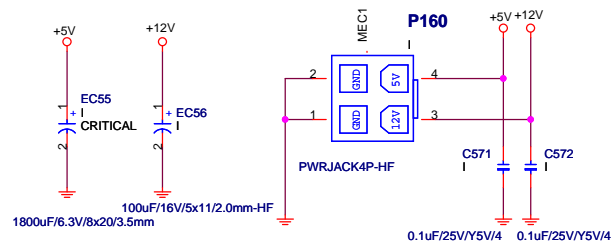
HP SCH P/N: 675886-000 (MSI MS-7782)

Size	Document Description	Rev
Custom	+12V_DUAL / +5V / +3.3V	X2
Date:	Sheet 51 of 63	

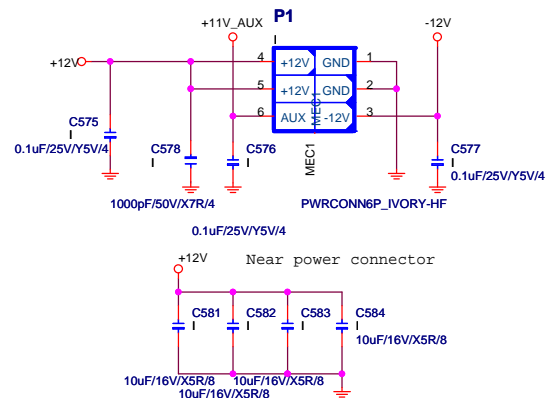
PN:N31-20510E1-F02



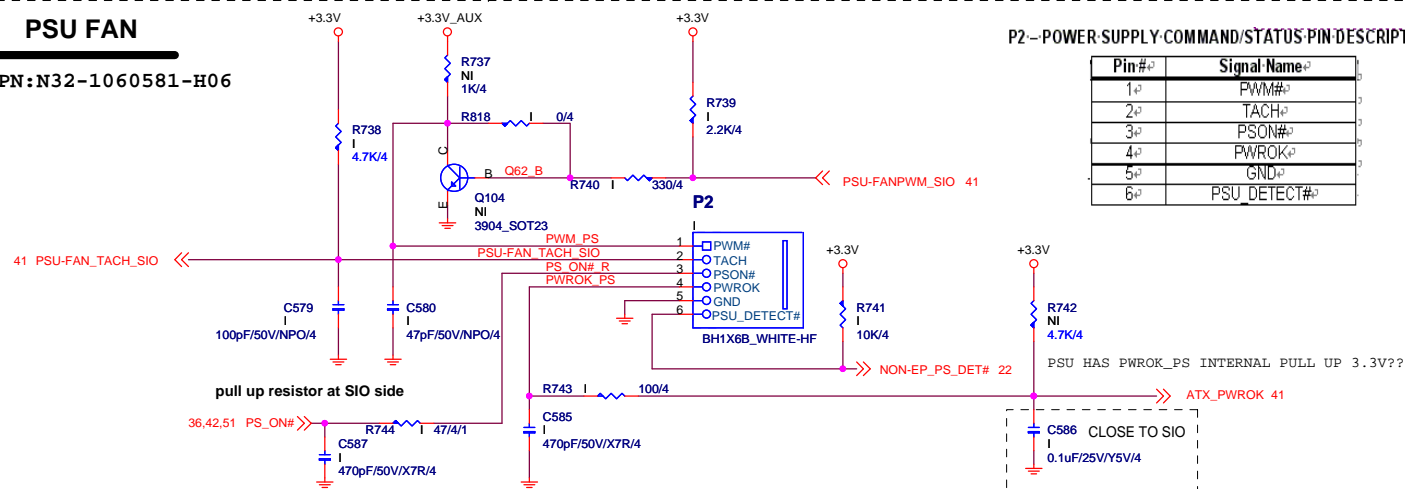
PN:N93-04M0451-H06



PN:N93-06M0241-H06



PN:N32-1060581-H06



**Release Date : Wednesday, November 23, 2011**



**MICRO-STAR INT'L CO.,LTD**

**HP SCH P/N: 675886-000 (MSI MS-7782)**

Size Custom	Document Description <b>Front Panel/ATX PWR CONN/SATA PWR CONN</b>	Rev X2
Date:	Sheet 52 of 63	

## 2

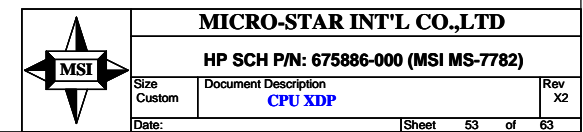
## DBG2



Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0 <sup>1</sup>	PREQ#	I/O	processor 4	4	OBSFN_C0 <sup>1</sup>	CFG[8]	I/O	processor
5	OBSFN_A1 <sup>1</sup>	PRDY#	I/O	processor 6	5	OBSFN_C1 <sup>1</sup>	CFG[9]	I/O	processor
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0 <sup>1</sup>	BPM#[0] / CFG[12]	I/O	processor 10	10	OBSDATA_C0 <sup>1</sup>	CFG[0]	I/O	processor
11	OBSDATA_A1 <sup>1</sup>	BPM#[1] / CFG[13]	I/O	processor 12	12	OBSDATA_C1 <sup>1</sup>	CFG[1]	I/O	processor
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2 <sup>1</sup>	BPM#[2] / CFG[14]	I/O	processor 16	16	OBSDATA_C2 <sup>1</sup>	CFG[2]	I/O	processor
17	OBSDATA_A3 <sup>1</sup>	BPM#[3] / CFG[15]	I/O	processor 18	18	OBSDATA_C3 <sup>1</sup>	CFG[3]	I/O	processor
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0 <sup>1</sup>	CFG[17]	I/O	processor 22	22	OBSFN_D0 <sup>1</sup>	CFG[4]	I/O	processor
23	OBSFN_B1 <sup>1</sup>	CFG[16]	I/O	processor 24	24	OBSFN_D1 <sup>1</sup>	CFG[5]	I/O	processor
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0 <sup>1</sup>	BPM#[4]	I/O	processor 30	30	OBSDATA_D0 <sup>1</sup>	CFG[10]	I/O	processor
29	OBSDATA_B1 <sup>1</sup>	BPM#[5]	I/O	processor 30	30	OBSDATA_D1 <sup>1</sup>	CFG[11]	I/O	processor
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2 <sup>1</sup>	BPM#[6]	I/O	processor 34	34	OBSDATA_D2 <sup>1</sup>	CFG[6]	I/O	processor
35	OBSDATA_B3 <sup>1</sup>	BPM#[7]	I/O	processor 36	36	OBSDATA_D3 <sup>1</sup>	CFG[7]	I/O	processor
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	PWRGOOD	I	system 40	40	ITPCLK/HOOK4	BCLK_ITP	I	processor
41	HOOK1 <sup>1</sup>	BP_PWRGD_RST#	I	system 42	42	ITPCLK#/HOOK5	BCLK_ITP#	I	processor
43	VCC_OBS_AB	VTT Voltage of the processor	I		44	VCC_OBS_CD	VTT Voltage of the processor	I	
45	HOOK2	TAPPWRGOOD	I	processor 46	46	HOOK6/RESET#	RESET_OBS#	I	processor
47	HOOK3	Open	NA		48	HOOK7/DBR#	DBR#	O	processor
49	GND	GND	NA		50	GND	GND	NA	
51	SLA <sup>1</sup>	SDA	I/O	system 52	52	TDO	TDO	I	processor
53	SCL <sup>1</sup>	SCL	I/O	system 54	54	TRStn	TRStn	O	processor
55	TCK1	Open	NA		56	TDI	TDI	O	processor
57	TCK0 <sup>3</sup>	TCK	O	processor 58	58	TMS	TMS	O	processor
59	GND	GND	NA		60	GND (XDP_PRESENT #)	--	NA	

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TO CPU



## PCH XDP

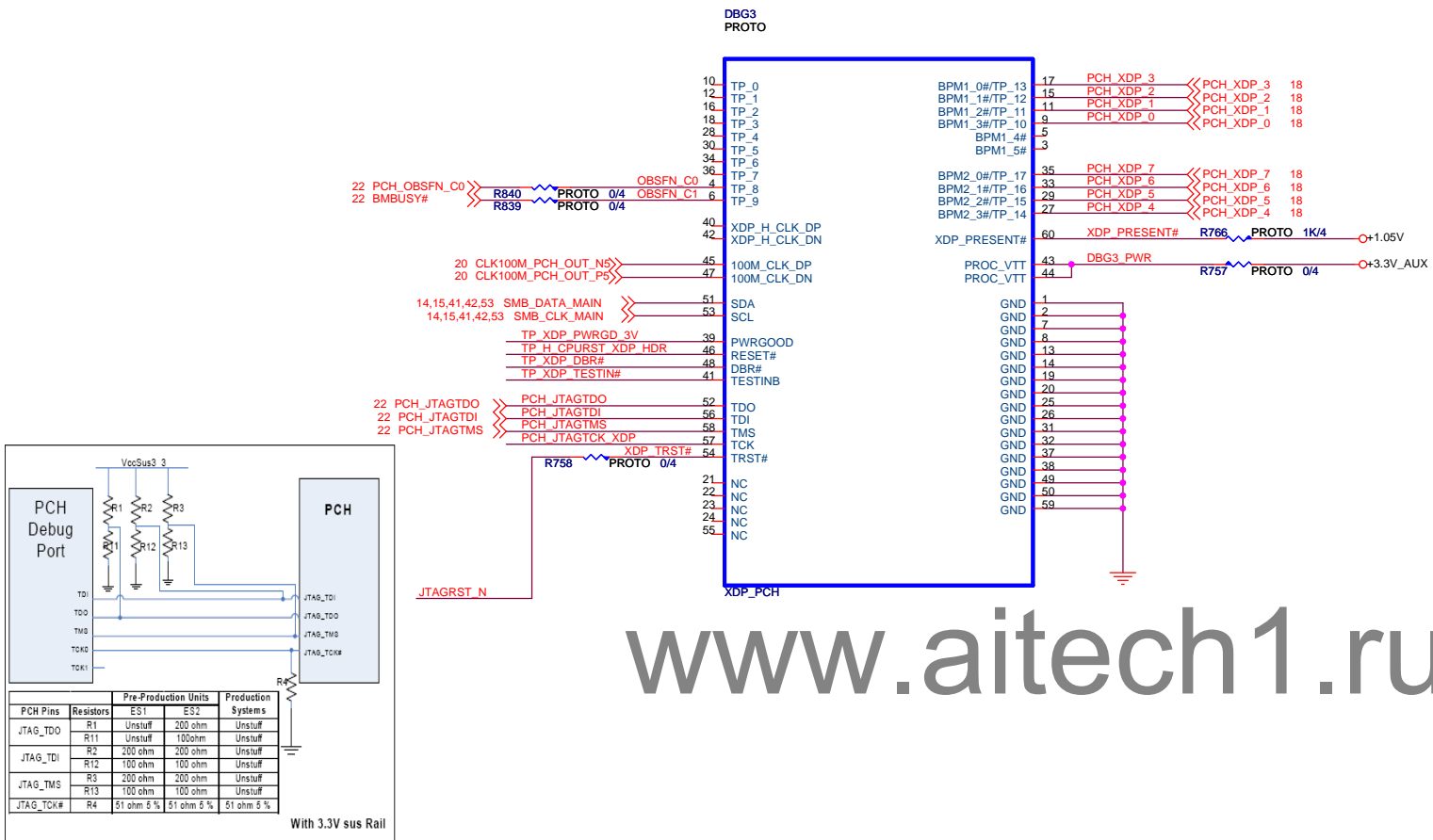


Table 4-1. PCH XDP Connector Pinout

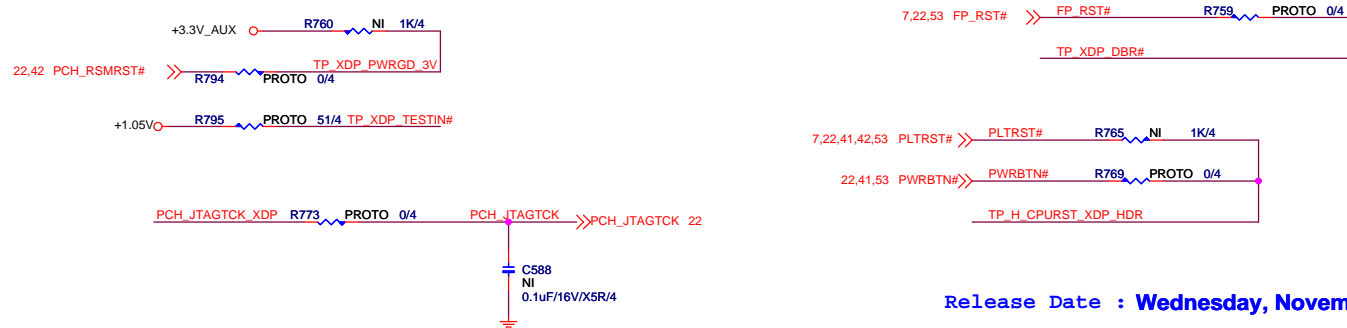
Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0	Open	NA		4	OBSFN_C0	GPIO28	I	PCH
5	OBSFN_A1	Open	NA		6	OBSFN_C1	BMBUSY# / GPIO0	I	PCH
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	OC0# / GPIO59	I	PCH	10	OBSDATA_C0	PCIECLKRQ2 # / GPIO20	I	PCH
11	OBSDATA_A1	OC1# / GPIO40	I	PCH	12	OBSDATA_C1	PCIECLKRQ1 # / GPIO18	I	PCH
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	OC2# / GPIO41	I	PCH	16	OBSDATA_C2	SATA0GP / GPIO21	I	PCH
17	OBSDATA_A3	OC3# / GPIO42	I	PCH	18	OBSDATA_C3	SATA1GP / GPIO19	I	PCH
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	Open	NA		22	OBSFN_D0	Open	NA	
23	OBSFN_B1	Open	NA		24	OBSFN_D1	Open	NA	
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	OC4# / GPIO43	I	PCH	28	OBSDATA_D0	SATA2GP / GPIO36	I	PCH
29	OBSDATA_B1	OC5# / GPIO9	I	PCH	30	OBSDATA_D1	SATA3GP / GPIO37	I	PCH
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	OC6# / GPIO10	I	PCH	34	OBSDATA_D2	SATA4GP / GPIO16	I	PCH
35	OBSDATA_B3	OC7# / GPIO14	I	PCH	36	OBSDATA_D3	SATA5GP / GPIO49	I	PCH
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	PWRGOOD	I	system	40	ITPCLK/HOOK4	Open	NA	
41	HOOK1	BP_PWRGD_ RST#	I	system	42	ITPCLK#/ HOOK5	Open	NA	
43	VCC_OBS_AB	3.3V	NA		44	VCC_OBS_CD	3.3V	NA	
45	HOOK2	Open	I		46	HOOK6/ RESET#	RESET#	I	system
47	HOOK3	Open	NA		48	HOOK7/DBR#	DBR#	O	system
49	GND	GND	NA		50	GND	GND	NA	
51	SDA	SDA	I/O	system	52	TDO	JTAG_TDO	I	PCH
53	SCL	SCL	I/O	system	54	TRSTn	Open	NA	
55	TCK1	Open	NA		56	TDI	JTAG_TDI	O	PCH
57	TCK0	JTAG_TCK	O	PCH	58	TMS	JTAG_TMS	O	PCH
59	GND	GND	NA		60	GND	GND	NA	

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### JTAG PULL HIGH/DOWN



### PCH XDP PWRGD/RESET



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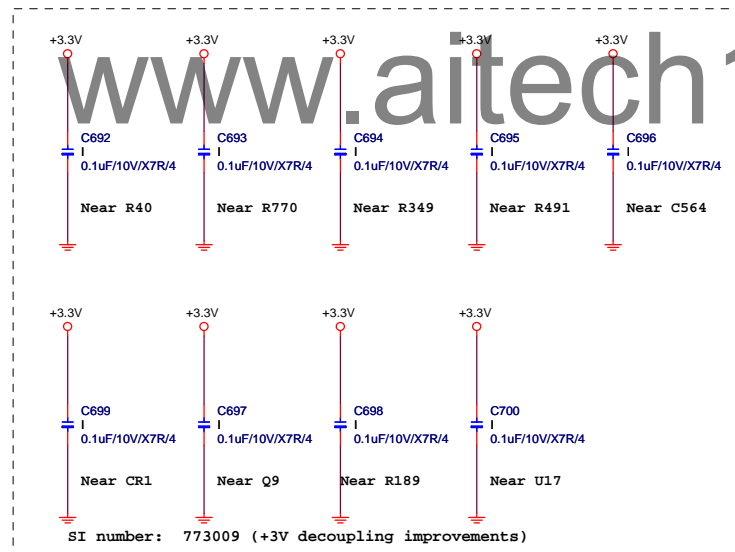
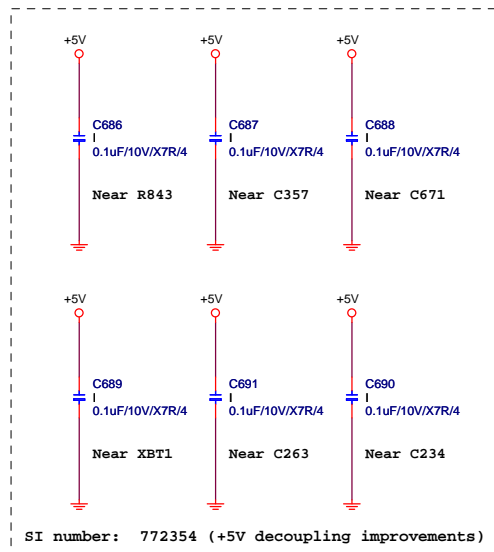
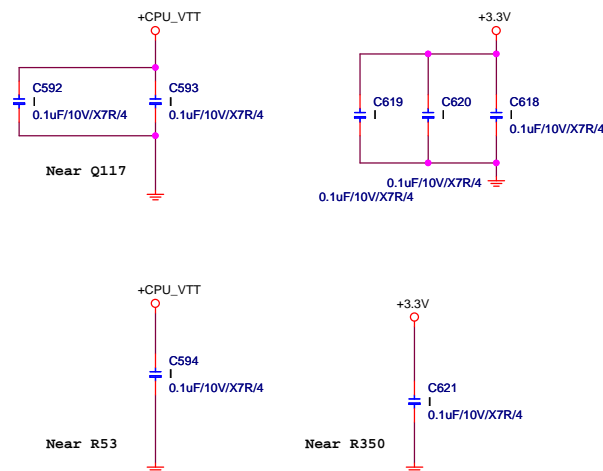
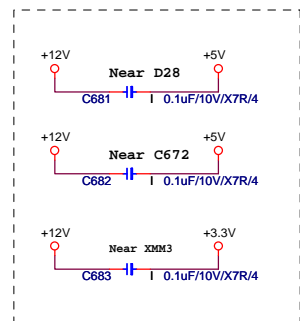


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# For EMI

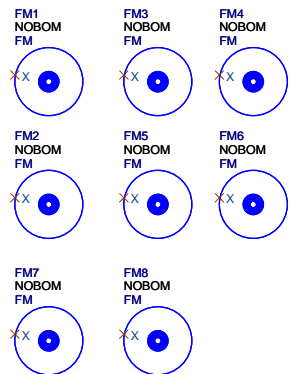


Release Date : Wednesday, November 23, 2011

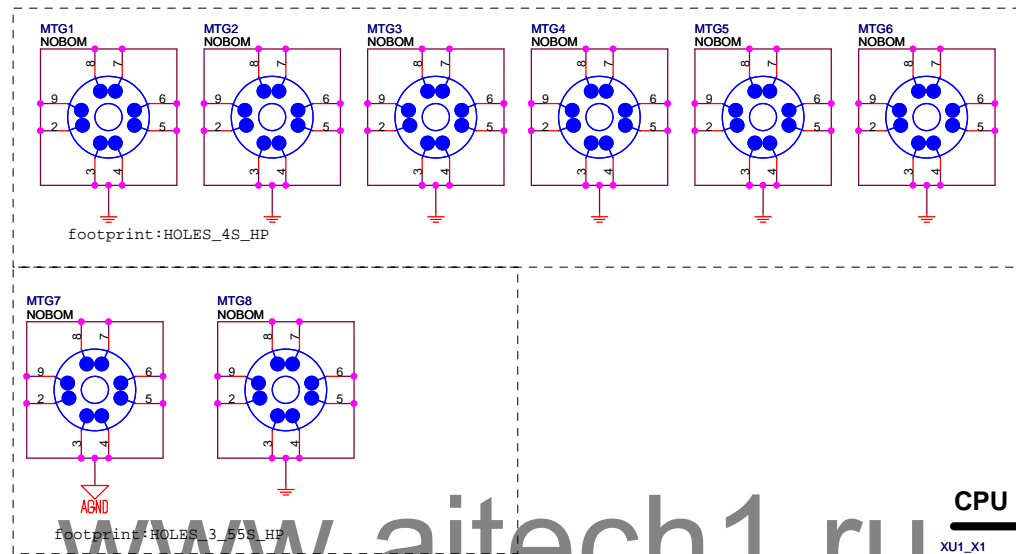


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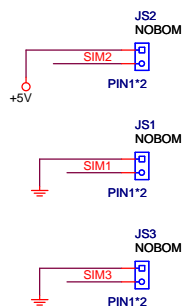
## Optics Orientation Holes



## Mounting Holes



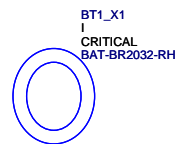
## Simulation



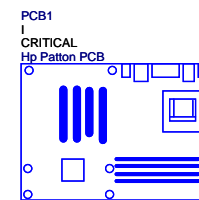
## NB/SB FAN/HEAT-SINK



## BATTERY

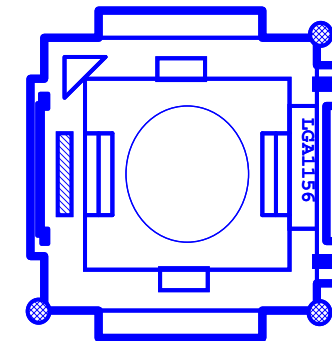


## PCB



## CPU SOCKET

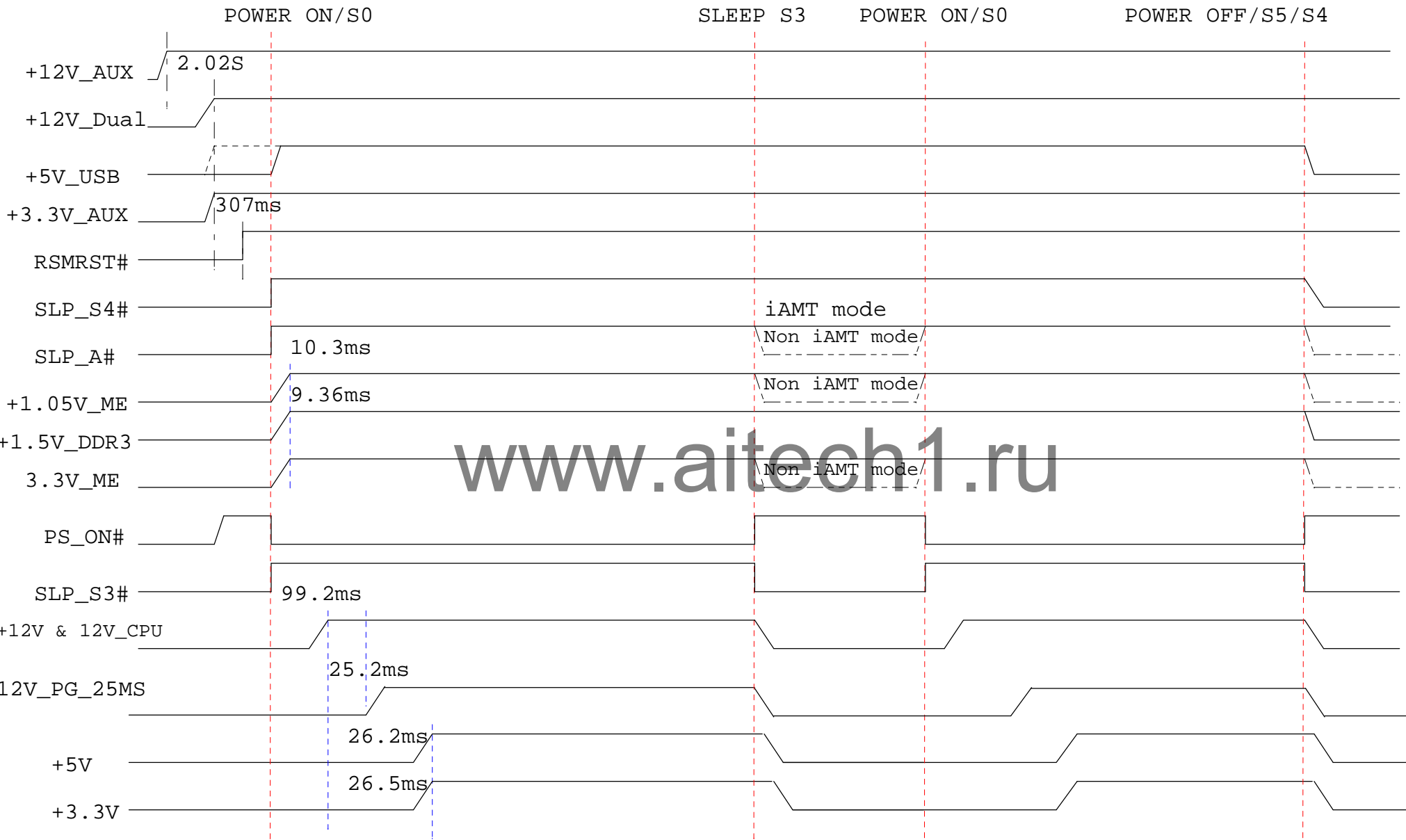
XU1\_X1  
CRITICAL  
CPU SOCKET



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Size Custom	Document Description BOM - Option Parts	Rev X2
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Size  
Custom

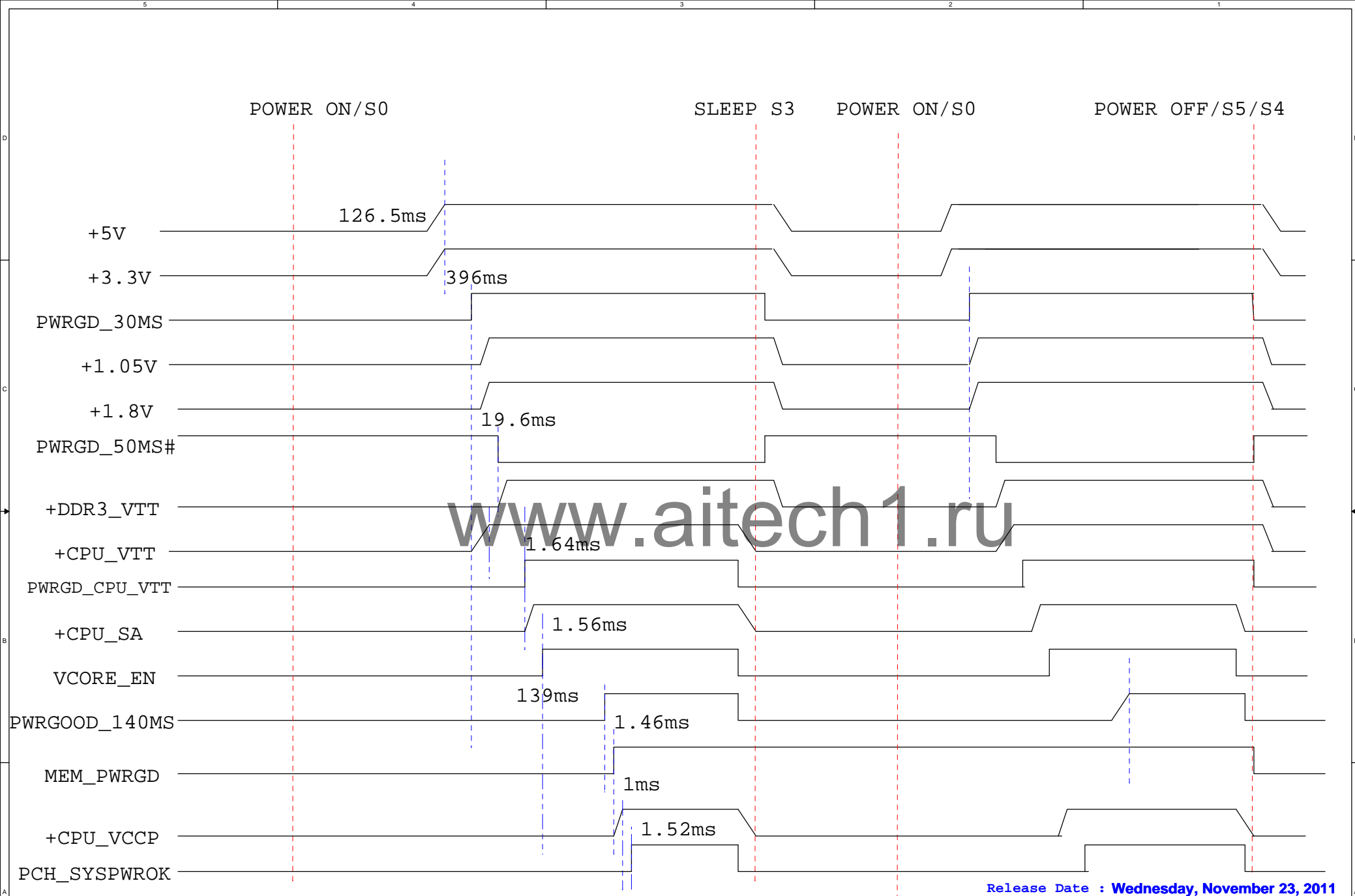
Document Description

Power Sequence-1

Rev  
X2

Date:

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Voltage Sequence Timing Requirements

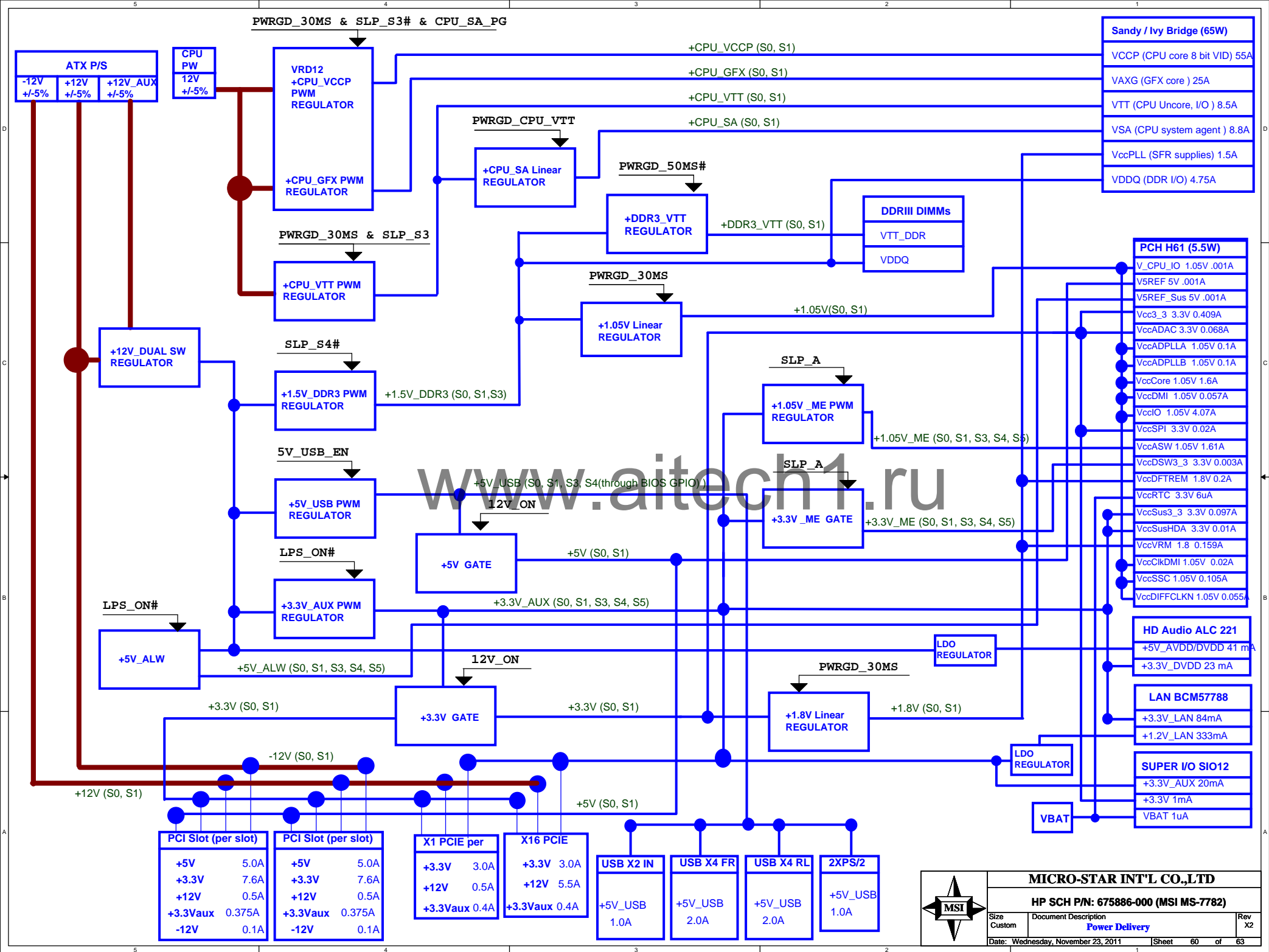


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- Notes:**
- 1. T16 = Time required for VTT to reach 90% of its level before VSA is asserted.
  - 2. T17 = Time required for VTT to reach 90% of its level before VCCPLL is asserted.

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	MICRO-STAR INT'L CO.,LTD	
	HP SCH P/N: 675886-000 (MSI MS-7782)	
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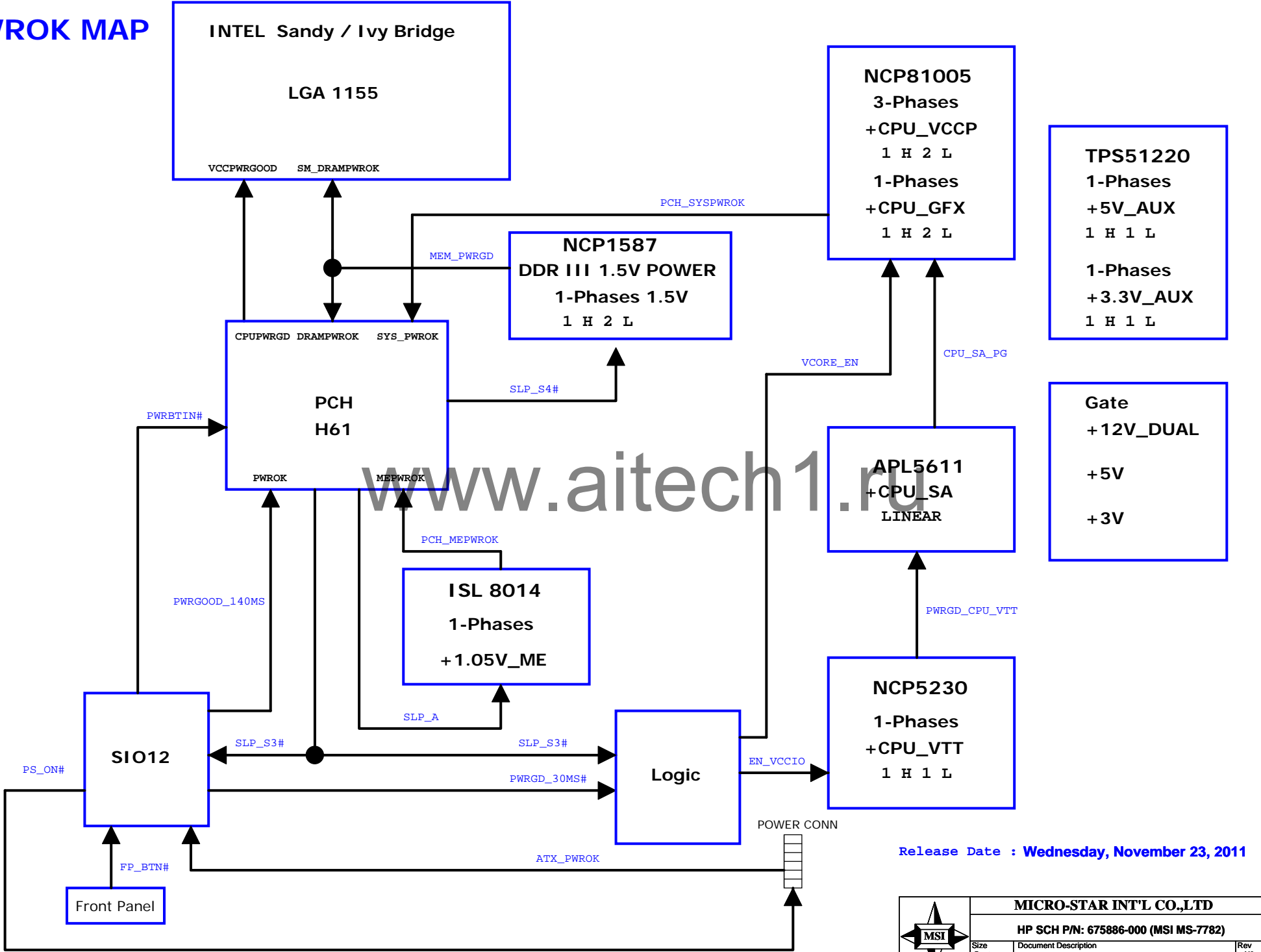


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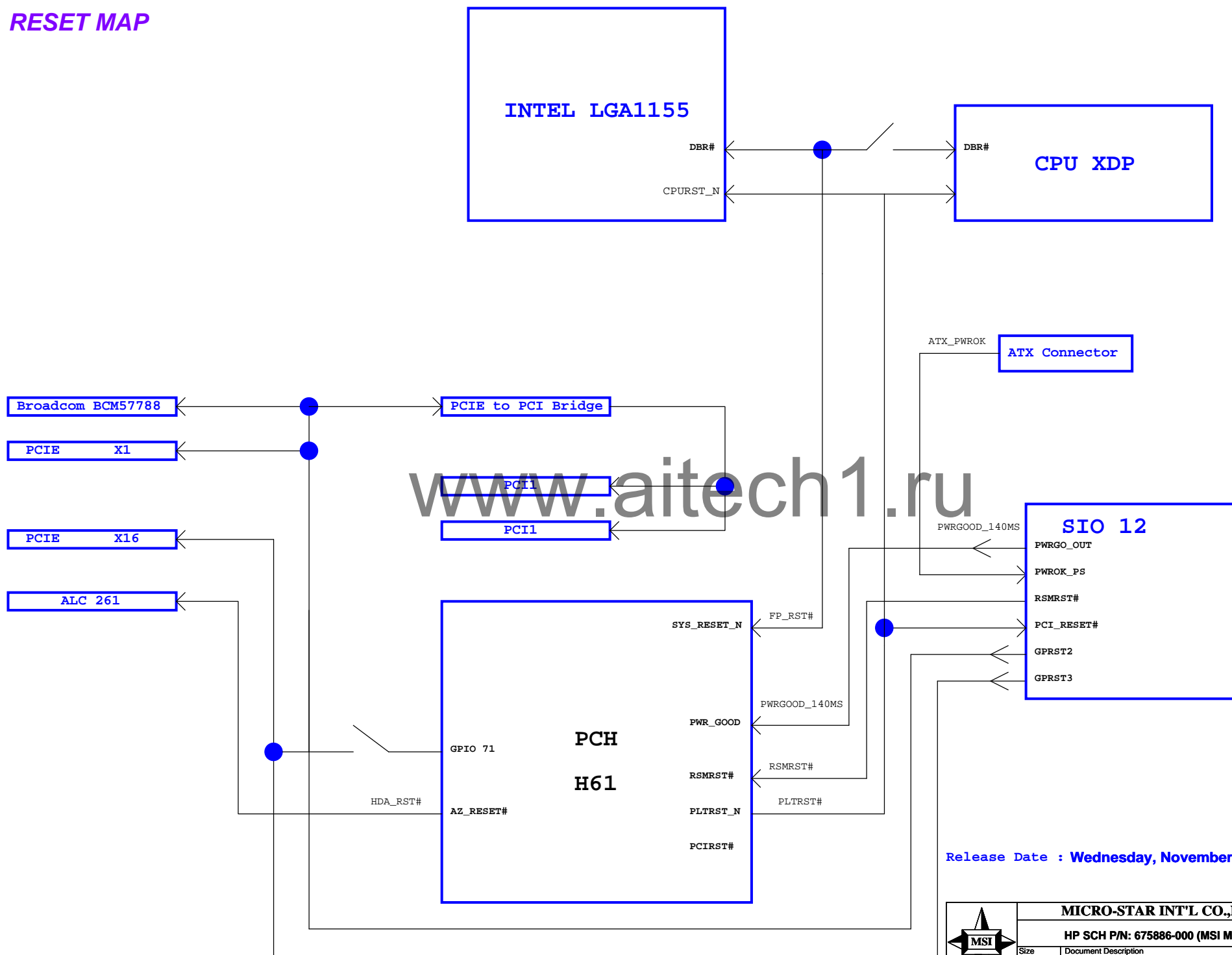
**HP SCH P/N: 675886-000 (MSI MS-7782)**

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PWROK MAP



# RESET MAP



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Size Custom	Document Description <b>RESET MAP</b>		Rev X2
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Patton 0A

2011/09/01 MS-7782 0A START

2011/09/27 MS-7782 0A Gerber Out

2011/09/30

PAGE55:+5V decoupling improvements (SI number: 772354)

PAGE55:+3V decoupling improvements (SI number: 773009)

2011/10/21

PAGE14,15:Data Mask has to connect to GND (SI number: 777180-2)

PAGE18:Modify DMI TX/RX circuit (SI number: 777197)

PAGE23:Modify DVI circuit (SI number: 777225)

PAGE36:XU19 pin5 must be connected to the E16 Pin 3 because SPI BOM can not be readed data (SI number: 777160)

2011/11/03

PAGE32:UUT is unable to power on if battery is removed;C240 is changed from 1uF to 4.7uF(SI number: 778258)

2011/11/10

PAGE13:- Modify Patton CPU power circuit to meet Intel CPU power transient test; C10,C11 have been changed from NI to I.(SI number: 780343)

PAGE46:- Modify Patton CPU power circuit to meet Intel CPU power transient test; C417=>220pF,R566=> 3.3K,R584=>7.15K,C443=>1500pF,C442=>820pF,R587=>8.66K (SI number: 780343)

PAGE47:- Modify Patton CPU power circuit to meet Intel CPU power transient test;EC34=>470uF (SI number: 780343)

PAGE48:- Modify Patton CPU power circuit to meet Intel CPU power transient test;C508=>0.01uF,C509=>0.01uF,C505=>2200pF,R629=>3.6K (SI number: 780343)

2011/11/14

PAGE33:Patton EVT1 RGB signals rise/fall time and pk-pk noise don't meet VESA 1.2 spec ;C246,C249,C252 have been chnage from 2.7pF to 4.7pF;L9~L14 have been changed from 33nH to 47nH. (SI number: 778268)

PAGE49:Add a 100uF cap to +1.05V\_ME power;EC48 =>100uF (SI number: 780770)

PAGE50:system power 3.3V change current to 22A solution ;Q86 =>MFS4921\*1,Q87=>MFS4937\*2 ,CHOKE12 => 1.5uH.EC52 => CAP SOLID,470uF\*2,R690 => 7.15K ohm,R687 => 15.8K ohm,EC49 =>,CAP SOLID,100uF (SI number: 780766)

2011/11/16

PAGE28:LAN\_AVDDL decoupling improvement;added C342,C343 near U10 pin 27,33 (SI number: 783475)

2011/11/17

PAGE42:Add LPC Debug Header;Added E17 (SI number: 780764)

PAGE42:SIO12 schematic review,strap pins pull down resistor value should be ;R879,R880,R881 have been changed to 4.7K ohm (SI number: 784070)

2011/11/21


PAGE13:Intel feedback "Some of the power decoupling caps (value and Qty) are not following Intel's recommendation " ,added 10uF :351,C352,C455,C456,C457,C458 (SI number: 784909)

PAGE24:Intel feedback "Some of the power decoupling caps (value and Qty) are not following Intel's recommendation " ,added 1uF:C701 (SI number: 784909)

PAGE47:Intel feedback "Some of the power decoupling caps (value and Qty) are not following Intel's recommendation " ,added 10uF:C344,C345,C347,C348; 270uF:EC38 (SI number: 784909)

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